SemiSouth

# White Paper WP-SS2

## JFET Gate Driver and Layout Considerations

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This white paper is intended to provide the reader with information about gate drive requirements and methods for driving the gate of a SiC JFET. Layout considerations have also been included to assist in yielding maximum performance.

## 1. Introduction

The unique structure of the SiC VJFET, Figure 1, manufactured by SemiSouth Laboratories requires specific needs from the gate drive if maximum performance is to be achieved. Each of the 3 main operating modes to be addressed is as follows:

- Steady-state conduction
- Turn-on
- Turn-off

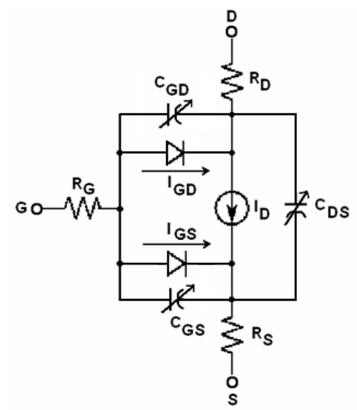



**Figure 1.** Schematic representation of VJFET device structure.

## 2. Steady-State Gate Drive Requirements

The required gate drive voltage for steady-state conduction is constrained to be between two different limits:

- High enough, so that the channel is adequately saturated.
- Not so high that the current that flows into the parasitic diode structures between gate and source draws so much current that the losses in the gate circuit are excessive.

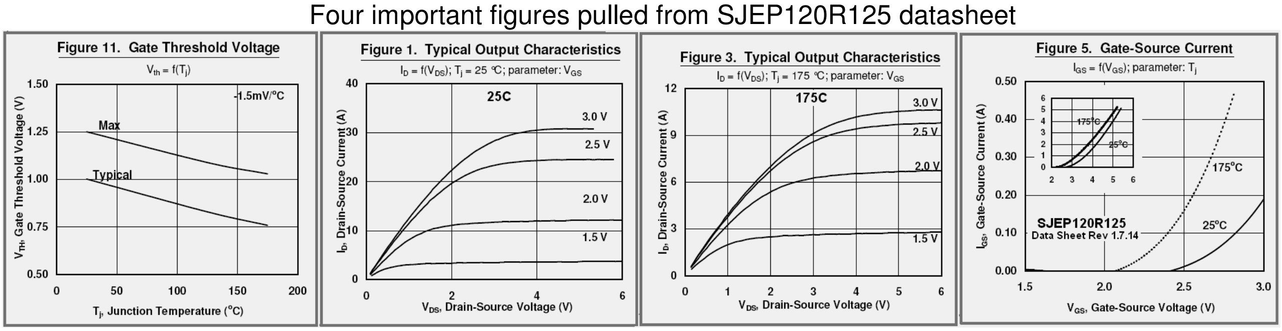
For adequate saturation of the channel the following factors are involved:

- Significant drain current only flows when the gate voltage exceeds the threshold voltage, $V_{GS(th)}$.
- $V_{GS(th)}$ has a negative temperature coefficient of approximately 1.5mV / C, as shown in *Figure 11* of the data sheet.
- The $R_{DS(ON)}$ decreases until $V_{GS}$ gets to between 2.5V and 3V, (depending upon temperature), as in *Figures 1 and 3* of the data sheet.
- Further increases in $V_{GS}$ beyond 3V yield no further reduction in $R_{DS(ON)}$.

The $I_{GS}$ vs. $V_{GS}$ characteristic of the parasitic diode that is part of the gate structure has the following features:

- Variation in device threshold voltage will still yield the same $V_{GS}$ vs. $V_{DS}$ characteristic. $I_{GS}$ vs $V_{GS}$ will vary slightly.
- If the gate current maintained at 100mA at both 25$^o$C and 175$^o$C, (ie. from a current regulated source), then at both temperatures the channel will be close to maximum saturation, (or minimum $R_{DS(ON)}$).

Four important figures pulled from SJEP120R125 datasheet



## 3. Turn-on

Conceptually, turn-on is similar to that for an IGBT or MOSFET, the faster the input capacitance is charged the faster the device will turn-on. Certain gate drive issues are also the same for the JFET as for other fast switching devices such as CoolMOS:

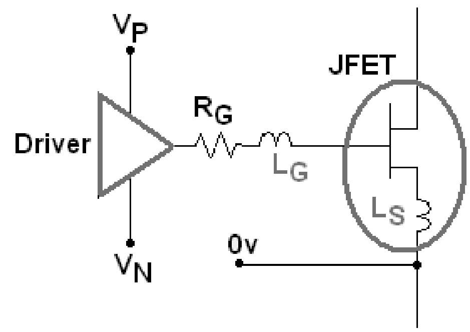



**Figure 2.** Gate Driver for Turn-on

- At turn-on, if the current is being commutated from a SiC freewheel diode, the diode's lack of a reverse recovery results in less damping in the circuit and a greater likelihood of high frequency oscillations in the $I_{DS}$ and $V_{DS}$ waveforms.
- For the TO-247 package, the gate and drain circuits share the common source lead and its associated leakage inductance $L_S$, Figure 2. Therefore any ringing on the $I_D$ waveform will be reflected onto the gate waveform. Hence it is important to minimize the ringing in the main drain circuit.
- Minimizing the distance between the gate driver and the JFET's gate terminal is essential in order to minimize $L_G$.
- A ferrite bead in series with the gate resistor can sometimes be used to reduce ringing in the gate circuit although sometimes at the expense of higher switching losses.

Additionally a few important factors are specific to the JFET must be addressed for best performance, especially for hard-switching:

- For an IGBT or MOSFET, the final gate voltage can be as high as 15V even if the gate threshold voltage is as low as 3V. However for the JFET, the final gate voltage is limited to ≤ 3v by the device's parasitic gate-source diode. As this is only ~2v above the threshold voltage, any parasitic ringing in the gate circuit has the potential to result in accidental turn-on or turn-off glitches. Therefore it is important to keep the ringing in the gate circuit minimized.
- For a given required turn-on speed a given peak gate current is required. The higher the driver's $V_P$ voltage, Figure 2, the higher the corresponding gate resistance $R_G$ is needed for a given gate current, and therefore the greater the damping in the gate circuit. Depending upon the particular gate drive circuit used, a higher $V_P$ voltage may however result in higher losses in the gate resistor that is used to limit the constant gate current required for steady-state conduction.
- For very fast switching, a high amplitude fast rising gate current pulse is required. Achieving an adequately fast rise time for this gate current pulse requires the gate leakage inductance, $L_G$, to be minimized.

## 4. Turn-off

Turn-off is relatively similar to that of an IGBT or MOSFET in that the faster the JFET's gate capacitor is discharged, the faster the JFET turns off. However, factors specific to the JFET must be addressed:

- The JFET does NOT have a turn-off "tail" current, like an IGBT. This lack of a tail reduces the turn-off losses, but also reduces the damping available at turn-off, resulting in high frequency ringing.

- A negative turn-off voltage is almost always required because the threshold voltage is so close to zero. Values of between -5V and -15V are commonly used. **NOTE:** that for a phase-leg configuration, (i.e. half bridge), the use of such a negative turn-off voltage is common practice with both IGBTs and MOSFETs in order to suppress the turn-on "glitch" that occurs on the gate of the device that is to be held off when the opposing device turns on. The lower the value of $L_G$, Figure 2, the more effective the negative gate bias is in suppressing this spurious turn-on glitch.
- If this turn-on glitch is not adequately suppressed, additional switching losses will result in both upper and lower devices. The addition of a small capacitor, (1 to 5nF), directly across the JFET's gate-source terminals can also be used if additional suppression is needed.

## 5. Example Gate Driver Circuits

Figure 3 below shows three possible gate drive circuits:

- **#1, The Simple R-C Circuit:** $R_{CL}$ is chosen to set the required gate current when the JFET is in conduction mode, and the $C_{BP}$ & $R_X$ circuit generates the required turn-on and turn-off gate current pulses. Even if $V_N$ is zero, unipolar driver, $C_{BP}$ will provide some degree of negative bias at turn-off to quickly pull the gate low for a fast turn-off transition. The duration of the negative bias will depend on the RC time constant of the gate driver.
- **#2, Dual-Driver Approach:** U1 generates a brief (~100nsec) high current pulse for fast turn-on. $V_P$ could be as high as 15V, allowing $R_{GON}$ to be as high as possible for the best damping. The high current pulse for the duration of the turn-on transient ensures that the JFET's gate is kept as far away from the 1V threshold as possible, to avoid any spurious gate transients from ringing in the gate circuit. U2 turns on at the same time as U1 to provide the steady-state gate current via $R_{COND}$, and turn-off via $R_{GOFF}$.
- **#3, Single High Current Driver:**, More applicable for higher current JFETs, but with similar operation to #2:
  - Q1 and Q2 providing the continuous gate current, in place of a more expensive driver IC.
  - Q1 & Q2 are supplied from a lower voltage power supply, (~6v), to reduce the losses in $R_{COND}$.

**NOTE:** In all the circuits shown in Figure 3, it is important to use a decoupling capacitor as close as possible to the U1 driver, to minimize any inductive voltage that might damage the driver.

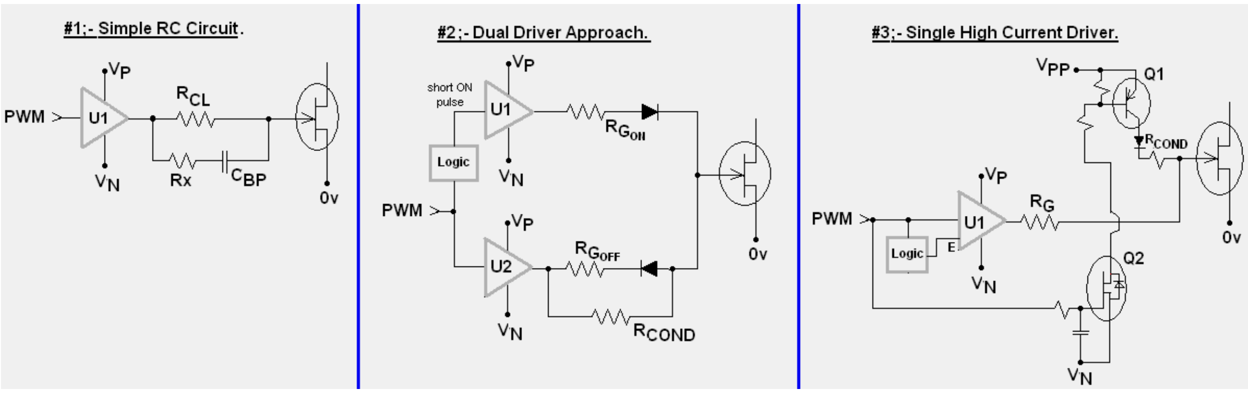



**Figure 3.** Example Gate Driver Circuits

6. **Optimizing the Main JFET–Diode Power Circuit**

As already mentioned in sections 3 and 4, the JFET's lack of the current "tail" at turn-off and the lack of reverse recovery when a SiC diode is used results in less damping and more ringing than an equivalent circuit utilizing a CoolMOS device plus a silicon diode. When very fast switching is desired, an R-C snubber across the DC bus in place of the typical film capacitor snubber can often yield cleaner waveforms, as was used in Figure 4 below. Notice also the reduction in ringing in both $I_D$ and $V_{GS}$ waveforms when the leakage inductance in the main JFET–diode circuit was reduced, Figure 6.

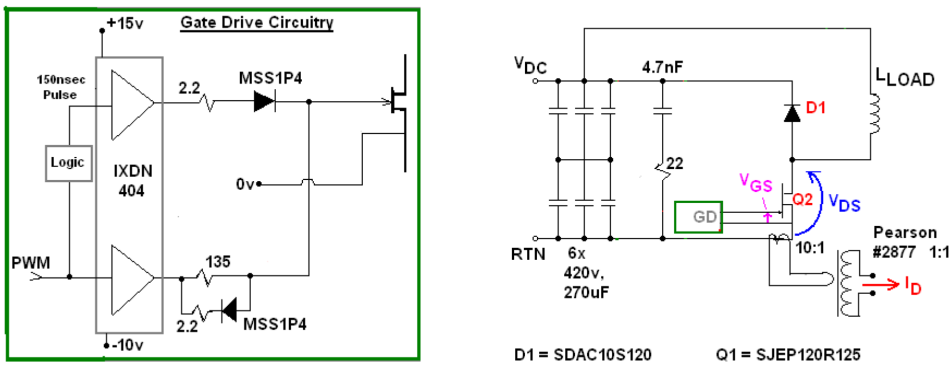



**Figure 4.** Schematic for gate circuit and power circuit.

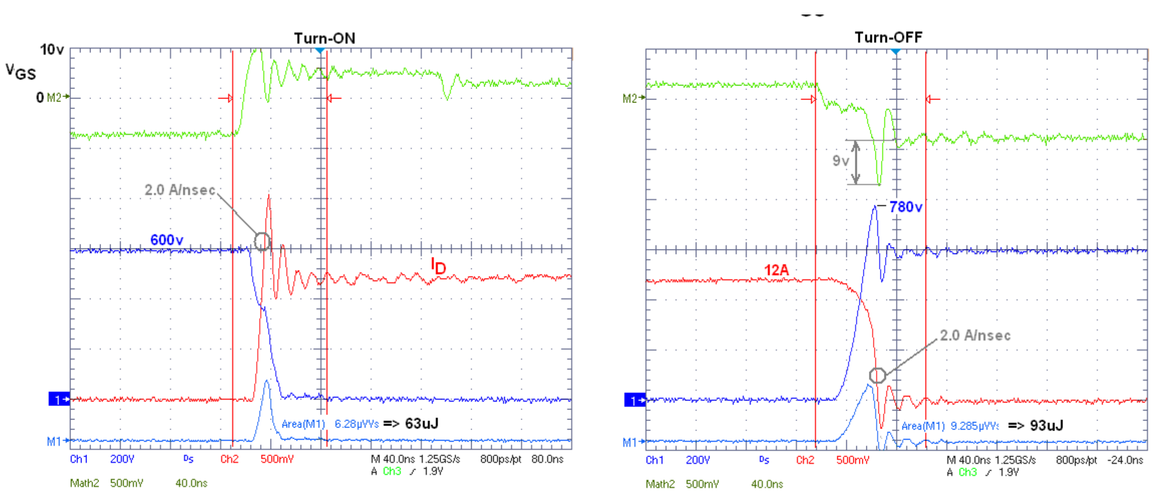



**Figure 5.** Q2 and D1 approximately 4cm apart. Significant ringing on both VGS and ID. $V_{DC}$ = 600V, $I_{PK}$ = 12A, Tj = 25$^{o}$C

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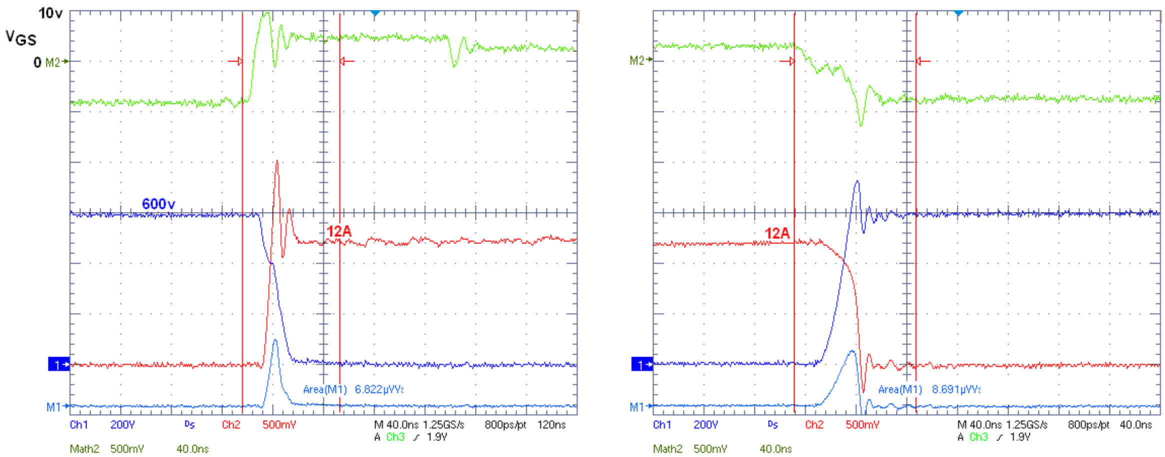


**Figure 6.** Distance between Q2 and D1 was reduced to ~1cm. Much less ringing on both $V_{GS}$ and $I_D$ than that of Figure 5.

## 7. Other Considerations

**Gate Driver Selection:**

- The gate driver IC or transistors must be rated for more than sum of the positive turn-on voltage and negative turn-off voltage.
- The gate driver's output resistance and peak current capability must be considered with reference to the peak gate current that is desired.
- The rise and fall times of the gate driver must be shorter than the required switching times of the JFET being driven.

**Gate Drive Layout:**

- To maximize the JFET's switching speed, the physical distance from the gate driver (IC or transistors) through any gate resistors and/or diodes to the JFET must be minimized in order to minimize the associated inductance. Ideally as low as 1cm as shown in this document.
- The decoupling capacitor (0.1 to 1uF) typically used across the $+V_P$ and $-V_N$ power supplies of the driver must be located as close as possible to the driver in order to protect it from over-voltages. Ideally this capacitance should be located immediately next to the driver.
- The bulk storage capacitors (1 – 10uF) on the $+V_P$ and $-V_N$ supplies must also be in close proximity to the gate driver.
- Non-inductive resistors must be used between the driver circuit and the JFET.