

Silicon Carbide Vertical Junction Field Effect Transistors Operated at Junction Temperatures Exceeding 300° C

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Abstract

4H-SiC vertical field effect transistors were fabricated. These devices, rated at 2A, 600V, were packaged and characterized at temperatures up to 300°C. At 300°C, DC forward current was reduced to 30% of the room temperature value when operated at a positive gate voltage of 2V. The maximum switching frequency ranged from 300kHz to above 1MHz at room temperature and increased by x2 when operated at 300°C. Parameters for modeling the devices in SPICE were also extracted and tabulated.

Key words: silicon carbide, high temperature, JFET, switching, SPICE

Introduction

Silicon carbide has long been promised as a solution for high temperature, high power applications where Si and GaAs cannot be used or require active cooling to operate. SiC Schottky diodes and MESFETs are already commercially available, and with the advancements in substrate quality and process technology that have been made in the last few years, other SiC devices for power applications will soon follow. It is likely that the next power device offering will be a unipolar transistor such a MOSFET or JFET. Unipolar devices have the particular advantage for power applications of having a negative temperature coefficient. That is, as temperature increases, the on resistance of the device increases. Because the current decreases as the device heats up, devices can be paralleled without concern of thermal runaway. The SiC JFET is also of particular interest because, unlike the SiC MOSFET, the JFET it is not so sensitive to the oxide interface and reliability issues. From a circuit design standpoint, however, some see the JFET as having the disadvantage of being a normally-on device. While JFETs can be made to be normally-off, higher current densities are available

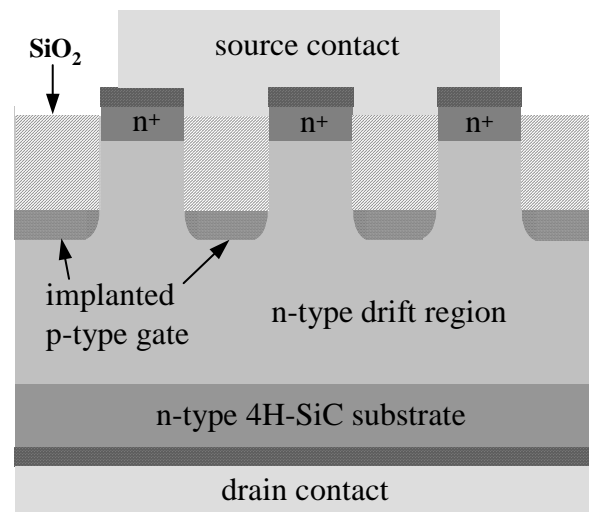


Fig. 1. The cartoon represents a cross-section view of the basic device structure of a 4H-SiC vertical trench JFET.

from normally-on devices. The pros and cons of using a normally-on SiC transistor are still under discussion [1]. In this work, we present DC and AC characterization at temperatures up to 300°C for normally-on 4H-SiC vertical JFETs as well as for

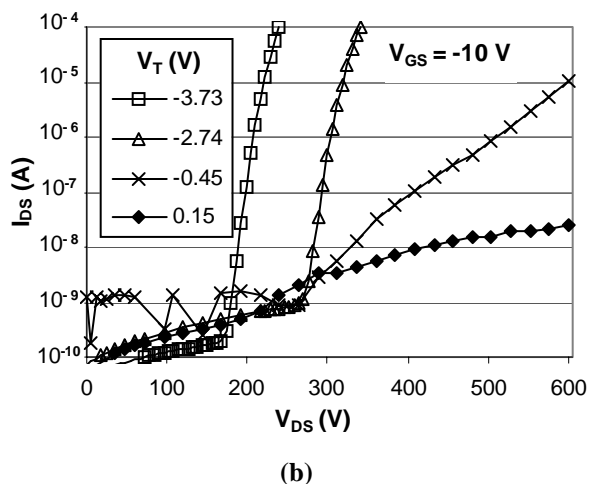
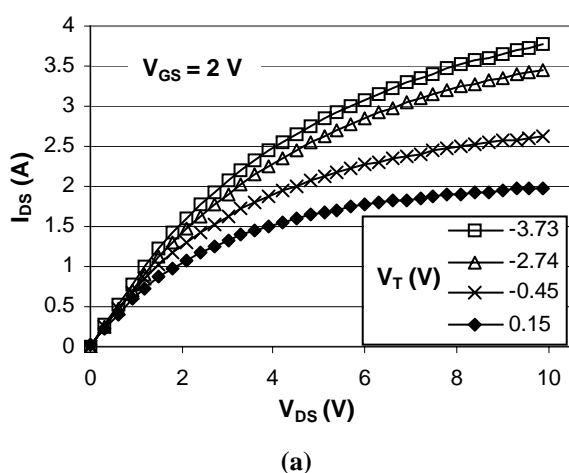


Fig. 2 Graph (a) shows I_{DS} vs. V_{DS} for $V_{GS} = 2$ V at 25°C for four VJFETs with various threshold voltages, V_T . Graph (b) shows blocking characteristics at $V_{GS} = -10$ V for the same four devices. (At $V_{GS} = -20$ V, all the above devices blocked 600 V at room temp.)

VJFETs that are “quasi-on”. It has been proposed that FETs falling in this quasi-on category may reduce some of the fears of using anything other than a normally-off transistor [2]. In addition to these electrical results, SPICE model parameters were extracted from the device characteristics using the Angelov model.

Device Description

The 4H-SiC VJFETs reported here were fabricated on n+ substrates with epitaxially grown n-type drift and channel layers. Trenches were dry etched and implanted with Al to form the p-type gates. The trenches were filled with oxide followed by the formation of ohmic contacts and contact pads. The basic device cross-section is shown in Figure 1. After dicing, the devices were mounted TO257 packages for testing.

DC Characterization

An advantage to the design presented here is that one can shift the threshold voltage negative or positive by widening or narrowing the nominal source finger width, respectively. Some of these devices were designed to have a negative V_T and therefore be normally-on at zero source-gate bias while others were designed to have a small negative or slightly positive V_T . In general, the more “on” a JFET is, the lower the specific on resistance. However, the more negative V_T , the more gate bias required to pinch the drain current off, especially at high drain voltages. Normally-off JFETs typically require very small negative gate biases to block the rated maximum voltage, but usually suffer from

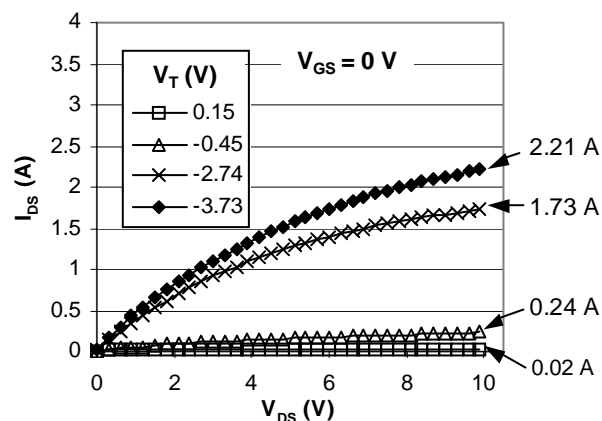


Fig. 3. The above graph shows I_{DS} vs. V_{GS} at zero gate bias for devices ranging from normally-on to quasi-on operation.

much lower saturation current than normally on devices. The trade-off between maximum current and blocking capability with relationship to V_T can be seen in Figure 2. Note in Fig. 2(a) that the device with the most negative V_T conducts nearly twice the current of the device that has the positive most V_T . Also note in Fig. 2(b) how the device with the most positive V_T has the lowest leakage current when blocking 600 V with a gate voltage of -10 V. On the other hand, the highest conducting device in the forward direction cannot block 200 V with the same -10 V on the gate. It should be stated, however, that the two devices showing premature breakdown in Fig. 2(b) are able to hold off 600 V with -20 V on the gate.

A compromise between a normally-on and normally-off FET is what has been called a quasi-on

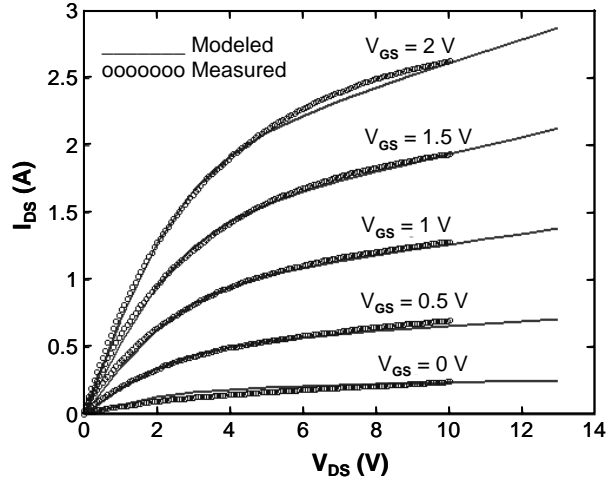


Fig. 4. The above graph compares measured data with modeled I-V curves for a SiC VJFET.

device. A quasi-on device is not fully pinched off with zero gate bias; however, the on resistance is high enough at $V_{GS} = 0$ V to limit the drain current enough to protect the device and circuit in the event of abnormal operating conditions such as a delay or failure in gate control [2]. As an example, consider Figure 3, which shows I_{DS} vs. V_{DS} for the same four devices in shown in Fig. 2, but with $V_{GS} = 0$ V instead of +2 V. The device that is the most normally on ($V_T = -3.73$ V) has a maximum $I_{DS} = 3.8$ A with $V_{GS} = 2$ V. At $V_{GS} = 0$ V, the maximum I_{DS} is reduced to 2.2 A – a reduction of only about 40% and still a considerable amount of current. Now consider the device with $V_T = -0.45$ V. With $V_{GS} = 2$ V it has a maximum drain current of 2.6 A which is almost 70% that of the $V_T = -3.73$ V device. However, at $V_{GS} = 0$ V the maximum drain current is reduced to 0.24 A – a reduction of 90%. From this example, it can be seen that a quasi-on device can provide good forward current while offering an elevated degree of protection from device or circuit malfunction.

SPICE models were developed for DC characteristics of the VJFETs using the Angelov model. Modeled I-V characteristics were in good agreement with measured data [Fig. 4]. The extracted model parameters for the device in Figure 4 are listed in Table 1.

Operating the devices at elevated temperatures resulted in an expected reduction of forward current. With sufficient gate voltage to turn the device on, the drain current for a fixed DC drain voltage exhibited an exponential decrease for temperatures from 25° to 250°C. The devices were limited to 250°C for these measurements to avoid melting the backside die-attach. Extrapolating a

Table 1. The Angelov parameters tabulated below, extracted from static data sets, can be used to make SPICE models for 4H-SiC JFETs.

Parameter	Description	Value
Ipk	Current at peak Gm	1.29
P1	I/V polynomial coefficient	0.66
P2	I/V polynomial coefficient	0
P3	I/V polynomial coefficient	0.09
B1	Sub threshold polynomial coefficient	-0.006
B2	Sub threshold polynomial coefficient	0
Vpk	Gate voltage at peak Gm	0.47
Vdb	Sub threshold voltage parameter	-176
Alpha	Drain I/V knee parameter	0.41
Lambda	Drain-source resistance parameter	0.059

fitted curve gives a drain current at 300°C of around 30% of the value at 25°C [Fig. 5(a)]. This result is in agreement with data reported by others from 4H-SiC lateral JFETs [3]. Leakage current in blocking mode increased up by up to two orders of magnitude. However, for devices having low room temperature leakage, leakage current out to the rated 600 V remained at an acceptable level at elevated temperatures as seen in Figure 5(b).

Drain current versus gate bias was measured with a constant V_{DS} of 10 V. Figure 6 shows I_{DS} - V_{GS} for a VJFET in semi log, (a), and linear scale, (b). The zero-temperature-coefficient, (ZTC) bias point is pointed out in Figure 6(a). The ZTC is defined as the gate voltage that produces the minimum change in drain current over the temperature range tested. It has been proposed that the ZTC can be utilized in the design of amplifier circuits for operation in temperatures from 25° to 300°C [4]. The inset table in Figure 6(b) shows the threshold voltage, V_T , for the device measured at the various temperatures. The magnitude of the negative shift in V_T was smaller the more “normally-on” the device. Specific on resistance, r_{on} , for the device in Figure 6 went from 6.8 $m\Omega \cdot cm^2$ at 25°C to 26.4 $m\Omega \cdot cm^2$ at 250°C. On

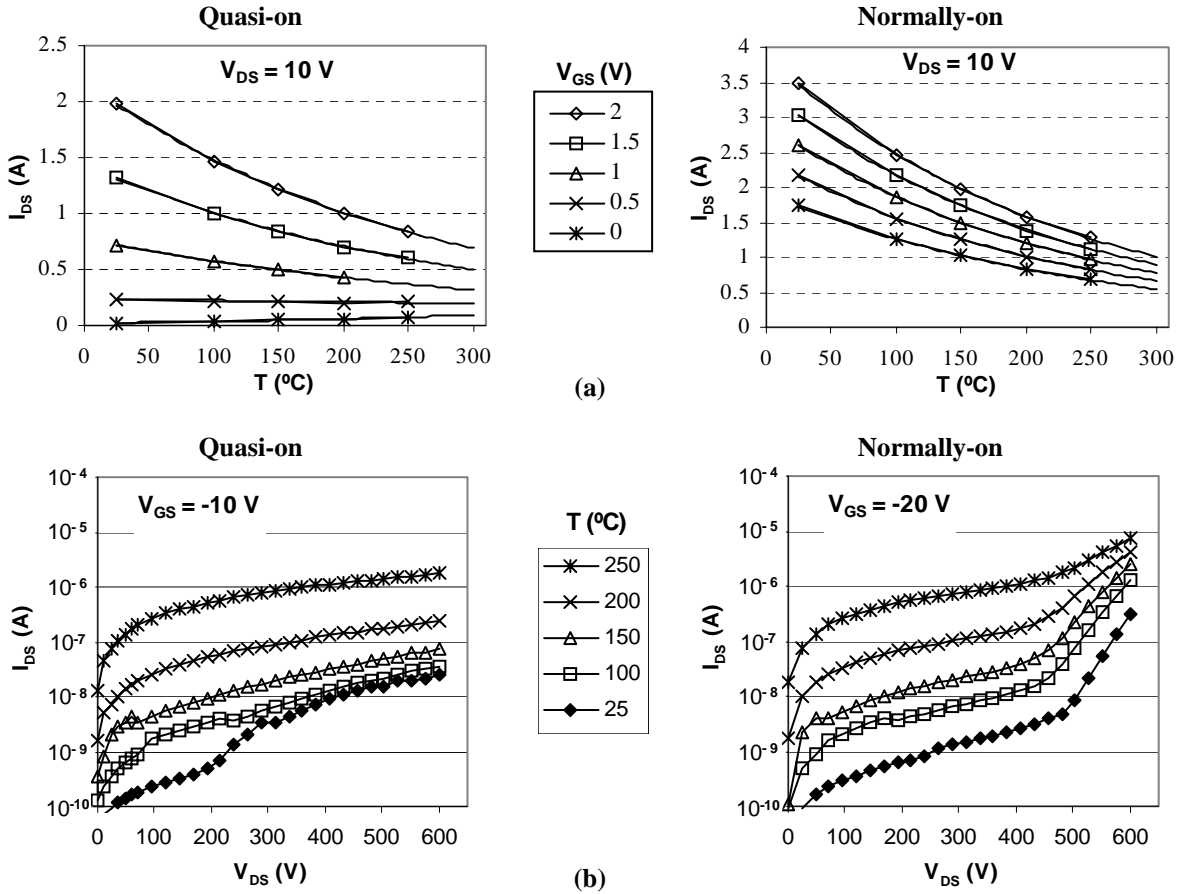


Fig. 5. Graph (a) shows drain current at $V_{DS} = 10$ V as a function of temperature for a quasi-on and normally-on VJFET. Graph (b) shows forward blocking characteristics from 25 to 250°C for a quasi-on VJFET and a normally-on VJFET for gate voltages of -10 V and -20 V, respectively.

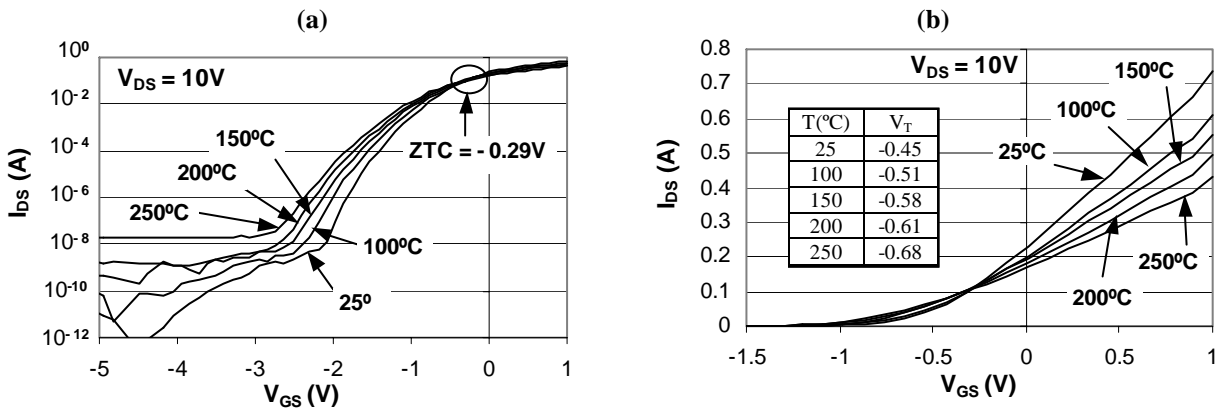


Fig. 6. The above graphs show I_{DS} vs. V_{GS} at $V_{DS} = 10$ V for a SiC VJFET at temperatures up to 250°C. The zero-temperature-coefficient operating area is pointed out in graph (a). The inset table in (b) gives the linear extrapolated threshold voltages for the various temperatures.

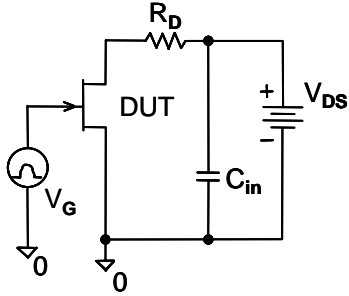


Fig. 7. This is a schematic of the test circuit used to measure the switching time of JFETs.

resistance was measured in the linear region of the $I_{DS}-V_{DS}$ curve at V_{DS} around 1 V and for a $V_{GS} = 2$ V.

Switching Measurements

The switching performance of SiC VJFETs was evaluated at case temperatures of 25°C through 300°C. The JEDEC standard test circuit used to perform switching time measurements is shown Figure 7. The only modification to the standard setup included the addition of 12" extensions added to the device leads. This allowed for device under test to be the only object subjected to the high temperatures. This is important because it is necessary that test circuit perform as characterized at room temperature during the high temperature analysis. For switching tests, V_{DS} was set at half the rated operating voltage of the device, i.e. 300 V.

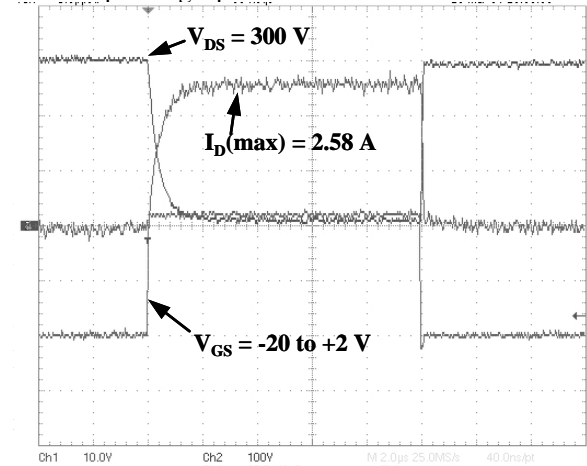
The first analysis performed allowed for the DUT (device under test) to operate in saturation mode for each trial. Figure 8 shows a graph of the gate voltage, drain voltage, and drain current as a function of time. As expected, the saturation current reduced with increasing temperature due to the increase in on resistance of the device. Also, a decrease in the rise time was observed indicating that the gate resistance decreased with temperature. A summary of the switching results from the device-limited setup is given in Table 2. Next, a larger load resistor was placed in the test circuit to limit the drain current to a maximum of around 0.5 amps thereby keeping the device from going into saturation. This setup produced much lower on voltages and therefore allowed the observation of the effects of temperature on switching more directly than with the device limited circuit. The results of the load-limited testing are shown in Table 3. The values for r_{on} from Table

Fig. 8. This switching curve was made with the JFET allowed to go into saturation.

3 are very close to the DC values measured at similar on voltages.

Conclusions

Packaged SiC vertical power JFETs have been fabricated and tested at operating case temperatures up to 300°C. Fully normally-on devices conducted over 3.5 Amps at room temperature with a corresponding specific on resistance of below 6



accurately model the devices in SPICE show that SiC JFETs should have a firm place in the world of high temperature – high power switching applications.

Table 2. The table below is a summary of the switching measurements made with the device allowed to go into saturation.

Temp (°C)	V _{GS} (V)	V _{DS} = 300 V				Von (V)	I _{DS} (A)	Pwr (W)	R _{on} (Ω)	r _{on} (mΩ*cm ²)	f (kHz)
		t _r (ns)	t _f (ns)	t _{d(on)}	t _{d(off)}						
25	0/-20	584	14.4	18.8	5.6	174	1.12	194.9	155.4	776.8	1606
	2/-20	1072	83.2	45.6	15.2	10.2	2.58	26.3	4.0	19.8	822
100	0/-20	480	26.8	14.4	7.2	190	1.04	197.6	182.7	913.5	1893
	2/-20	520	28.4	24.4	10.8	42	2.38	100.0	17.6	88.2	1714
200	0/-20	452	19.2	12	6.4	212	0.88	186.6	240.9	1204.5	2042
	2/-20	232	26	14.8	7.2	118	1.66	195.9	71.1	355.4	3571
300	0/-20	540	41.6	13.2	7.2	220	0.76	167.2	289.5	1447.4	1661
	2/-20	128	36	12.8	6.4	168	1.21	203.3	138.8	694.2	5459

Table 3. The table below is a summary of the switching measurements made with the current limited to around 0.5 Amps.

Temp (°C)	V _{GS} (V)	V _{DS} = 300 V				Von (V)	I _{DS} (A)	Pwr (W)	R _{on} (Ω)	r _{on} (mΩ*cm ²)	f (kHz)
		t _r (ns)	t _f (ns)	t _{d(on)}	t _{d(off)}						
25	0/-20	2360	168	80	36.8	22	0.496	10.9	44.4	221.8	378
	2/-20	516	182.4	37.6	80	0.68	0.548	0.4	1.2	6.2	1225
100	0/-20	920	111.2	43.3	18.4	27.6	0.516	14.2	53.5	267.4	915
	2/-20	184	125.6	23.6	30.4	1.36	0.564	0.8	2.4	12.1	2750
200	0/-20	513.6	148.8	20.8	13.6	40	0.484	19.4	82.6	413.2	1435
	2/-20	134.4	131.2	19.2	19.2	3.2	0.564	1.8	5.7	28.4	3289
300	0/-20	536	175.2	23.2	11.2	64	0.444	28.4	144.1	720.7	1341
	2/-20	128	155.2	17.6	16	5.8	0.564	3.3	10.3	51.4	3157

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