

SiC JFET Gate Driver Design for Use in DC/DC Converters

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Abstract — Even though there is increasing interest in silicon carbide (SiC) JFETs, the fact that they are most commonly normally on devices intimidates some designers. Therefore it is important that appropriate gate driver circuits are also introduced to ease the negative concerns associated with a normally on device. By introducing inherently safe gate driver circuits specially designed for the SiC JFET, it will be possible to prove that designing applications using SiC JFETs is not as complicated as some may think. Therefore, this paper provides a follow-up to previous work that introduced an inherently-safe gate driver design for a buck converter [1]-[2]. In this paper, another gate driver is introduced that is not only inherently-safe but also provides an isolated solution ideal for a variety of applications. This gate driver is a practical solution for driving both normally-on and enhancement mode SiC JFETs in virtually all power converter topologies.

I. INTRODUCTION

As SiC JFETs continue to generate interest as switching devices for power electronics, the need for simple, inherently-safe gate drivers is also growing. While many designers are initially impressed with the possibility of operating in high ambient temperature with relaxed cooling requirements, and the promise of higher power density, the reputation of being a normally on device is still a major concern. This paper examines a new, simple, inherently-safe gate driver design to show that the use of SiC JFETs in any application is not a difficult task.

The purpose of this paper is to follow up earlier work that introduced an inherently-safe gate driver design for a buck converter. In this paper, another gate driver is introduced that is not only inherently-safe but also provides isolation from the main control circuit. This gate driver is a practical solution for driving both normally on and enhancement mode SiC JFETs in virtually all power converter topologies. The magnetic isolation also makes it ideal for high-side gate drivers in half- and full-bridge converter.

II. GATE DRIVER DESIGN WITH RESULTS

Previously published work introduced a simple technique for driving a SiC JFET in a buck converter that utilized the output voltage as the negative bias required to turn-off the device [1]. This paper introduces a technique for use in

converters in which the source terminal of the main switching device is either floating or tied to ground. This design self generates the negative bias required to turn-off the device, while inherently finding the cut-on voltage required by the JFET without excessively forward biasing the gate-source diode. Fig. 1 contains a schematic of the gate driver design. This design takes advantage of the diode structure of the gate-source terminal in order to self generate the negative bias necessary for blocking the full rated voltage of either normally on or enhancement-mode (normally off) SiC JFETs that exhibit bias-enhanced blocking [1]. Like previous work, this design also uses a standard commercially available ASIC commonly used for driving MOSFET.

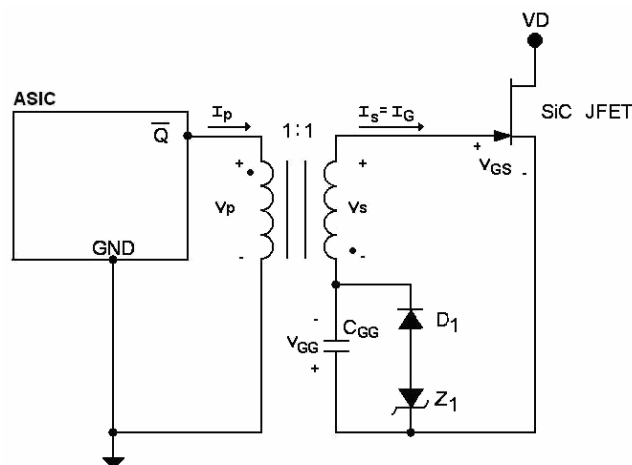


Fig. 1. Proposed gate driver design

For the design shown in Fig. 1, isolation is provided by the one to one flyback transformer used to reflect the inverse of the complementary output from the ASIC. In the event a complementary output is not available on the ASIC, a simple inverter circuit composed of a single PNP BJT can be used to apply the inverted chip output to the primary side of the flyback transformer.

A simple voltage loop governs the gate-source terminal of the JFET throughout the switching period,

$$V_{GG} - V_S + V_{GS} = 0 \quad (1)$$

From this we get:
$$V_{GS} = V_S - V_{GG} \quad (2)$$

The characteristic waveforms that explain the operation of this circuit are shown in Fig. 2. At time t_0 , the inverted output from the ASIC transitions to a high logic state applying V_{CC} across the primary winding of the transformer. From time t_0 to t_1 , the necessary energy required to drive the JFET into conduction is stored in the core of the transformer. V_S results in a negative value (flyback voltage) and thus a voltage $V_{GS} = -V_S - V_{GG}$ is applied to the gate-source terminals of the JFET. At time t_1 , the ASIC output voltage returns to a logic low state and flyback action is initiated. Between times t_1 to t_2 ($= t_{on}$ for the JFET), V_S flies back to the positive (according to the polarity noted in Fig. 2) voltage necessary to overcome the negative V_{GG} voltage by a difference equal to the cut-on voltage of the JFET, typically +3 V, so as to commutate the transformer magnetic current from the primary to the secondary. The gate voltage will remain 'high' until the gate current is reduced to zero indicating that the core is completely reset (or until the next switching transient is initiated by the ASIC if critical or continuous conduction is desired). At this time, noted as t_2 , V_S collapses to zero and the device is pinched off by the negative voltage V_{GG} applied to the gate of the JFET, $V_{GS} = -V_{GG}$. The energy storage capacitor will continue to hold the device in pinch off until the next switching transient is initiated, at time t_3 , by the ASIC. Note that if the gate driver is operating in critical or continuous conduction mode, as previously mentioned to be possible, then times t_2 and t_3 are the same instance. In effect, the gate driver is a very small flyback converter that uses the gate-source junction of the JFET as the freewheeling output diode.

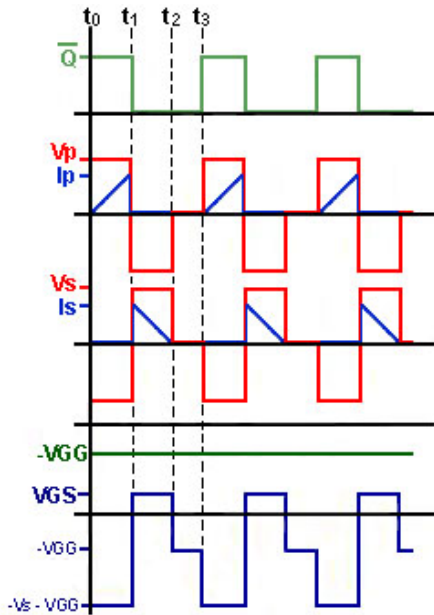


Fig. 2. Representative gate driver waveforms.

After designing the transformer each of the time intervals noted in Fig. 2 can be quantified using inductor voltage equations,

$$V_P = L \Delta i / \Delta t_P \quad (3)$$

$$V_S = L \Delta i / \Delta t_S \quad (4)$$

Since a unity turns ratio transformer is used, the primary and secondary inductance values will be equal. This also dictates that the peak current for each winding will be equal and since the core will be allowed to reset completely during each switching period, the value of Δi is the same for both (3) and (4). As previously mentioned, switch characteristics along with the main converter design will determine the values of t_S ($= t_{on}$ for the JFET), V_{GG} , and V_S . The value of Δi is also selected based on the DC characteristics of the device such that C_{GG} is recharged without over driving the gate-source diode of the JFET. As seen in Fig. 1, a zener and pn diode combination are used to clamp C_{GG} at the desired V_{GG} voltage and commutate any additional transfer of energy beyond what the capacitor requires. Knowing these parameters, L is determined from,

$$L = V_S \Delta t_S / \Delta i \quad (5)$$

Then,

$$t_P = V_S t_S / V_P \quad (6)$$

In the case that t_S plus t_P does not equal the full switching period, the flyback transformer will operate in discontinuous conduction mode and during the interval equal to the difference between t_S and t_P $V_{GS} = -V_{GG}$, as noted by time t_2 to t_3 in Fig. 2. However, as long as V_{GG} is maintained at the negative bias required for blocking the maximum drain voltage applied by converter, continuous variable duty ratio control is possible by adjusting the t_2 to t_3 time interval. Fig. 3 and 4 are screenshots of a working gate driver prototype operating in critical conduction mode with a 600V, 5A SiC JFET.

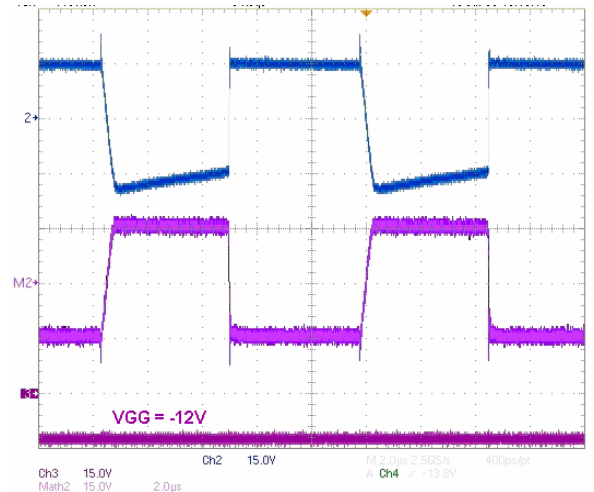


Fig. 3. V_P (top), V_S (middle), and V_{GG} (bottom) voltages. Gate driver switching frequency is 100 kHz.

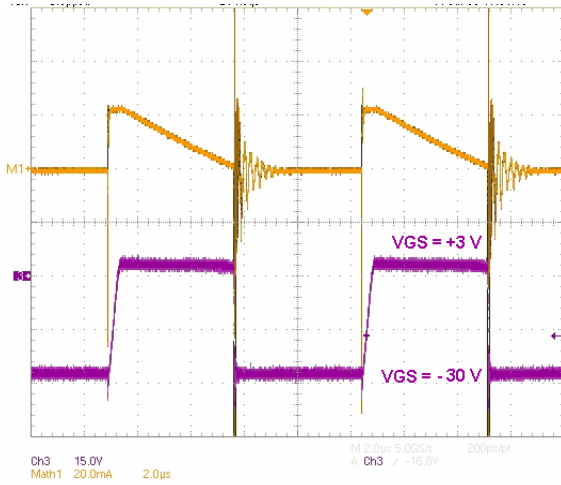


Fig. 4. I_G (top) and V_{GS} (bottom). Gate drive switching frequency is 100 kHz.

III. INHERENT SAFETY

Fig. 3 and 4 show that a fast switching gate driver circuit resulted and is capable of driving a SiC JFET while providing inherent safety. Based on the schematic shown in Fig. 1, inherent safe is provided by a combination of device and circuit design. For converters that experience different levels of static and dynamic voltage stress a quasi-off device could be selected. For example, power converters such as the boost and resonant reset forward converter, the switch is exposed to a static dc input voltage during start-up or any instance of gate driver failure, then during normal switching operation a dynamic voltage stress greater than the input voltage is endured. For either example, a quasi-off device can be selected such that it is capable of blocking the dc input voltage at $V_{GS} = 0V$ and block the greater dynamic stress during normally switching operation at which time an appropriate negative bias can be derived. For any case where a fully normally on device is used, addition start-up circuit would be designed to ensure that any time a gate driver failure occurs, the device is indefinitely pinched off beyond the protection provided by the gate driver.

Focusing on the gate driver circuit alone, C_{GG} is sized appropriately to hold the device in pinch off for a defined amount of time. If the ASIC were to fail and a constant low output voltage is experienced across L_p , L_s would also equal zero and V_{GS} would be equal to $-V_{GG}$ until C_{GG} is completely discharged. This discharge time is designed for based on the needs of the application. If the failure occurs while using a quasi-off device, as C_{GG} begins to discharged any high voltage transients should have completely ceased and the device would be capable of indefinitely blocking the input DC voltage long after C_{GG} has completely discharged, $V_{GS} = 0V$. For the case of a normally on device, additional start-up and protection circuitry would be required to ensure isolation between the input DC voltage and remaining circuit was

established before C_{GG} is discharged to an unsafe level, i.e. below the value required to block the full input voltage.

IV. DEVICES AND APPLICATIONS

SiC JFETs can be manufactured in three different conduction types; fully normally off (capable of blocking $BV_{DS(max)}$ at $V_{GS} = 0V$), quasi-off (previously referred to as bias-enhanced capable of blocking half $BV_{DS(max)}$ at $V_{GS} = 0V$), and ‘hard’ normally on (unable to block any amount of voltage at $V_{GS} = 0V$). There exists trade-offs between each of the three conduction types mostly evident in the forward current ratings and specific on resistance. Due to the structure of the device the normally on device yields the greatest forward current ratings and lowest on resistance. The quasi-off device that is design to block up to half of the maximum blocking capabilities at $V_{GS} = 0$, typically results in 1.5x reduction in forward current with the normally off device demonstrating greater than 2x reduction in forward current ratings. Because of the large reduction in conduction current capabilities of the normally off device, the normally on and quasi-off devices are more strongly promoted. Fig. 5 and 6 provide typical BV_{DS} vs V_{GS} curves for both a normally on and quasi-off device, respectfully, to illustrate the negative bias requires for both types of devices.

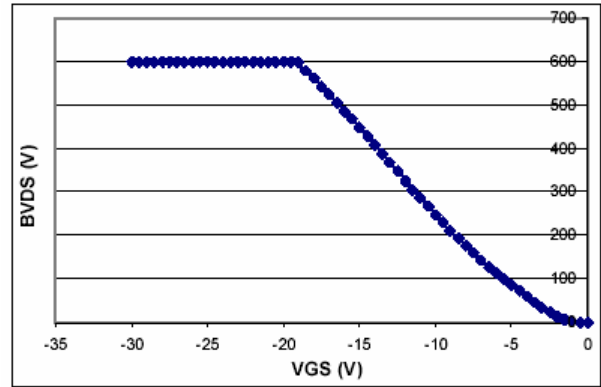


Fig. 5. BV_{DS} vs V_{GS} curve for a normally on SiC JFET [3].

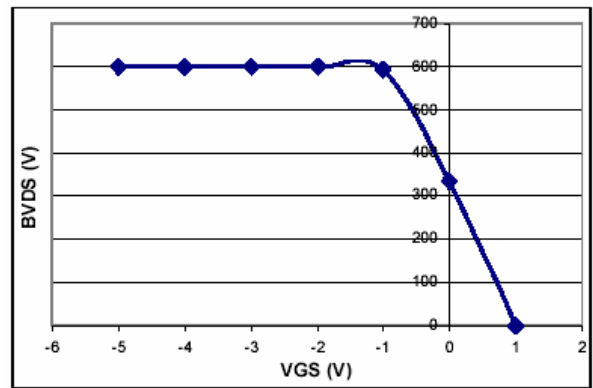


Fig. 6. BV_{DS} vs V_{GS} for a quasi-on SiC JFET [3].

Fig. 7 provides a schematic diagram of the resonant reset forward converter that was prototyped using the gate driver presented in this paper. For this design the ASIC was purposefully powered off of the output voltage. This approach eliminates the need for any optocouplers commonly used to relaying feedback signals to the primary side, devices known for been limiting factors for reliability. The flyback transform then provides the isolation required to drive the gate of the JFET on the primary side of the power converter. Resulting waveforms from the offline (170 VDC) to 24V resonant reset forward converter prototype are shown in Fig. 8.

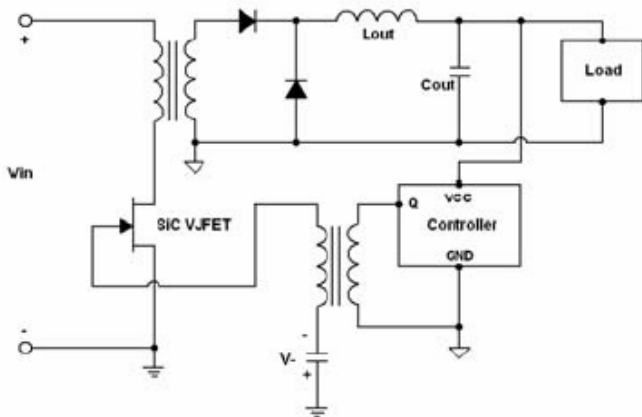


Fig. 7. Schematic of an inherently safe resonant reset forward converter using the presented gate driver circuit [3].

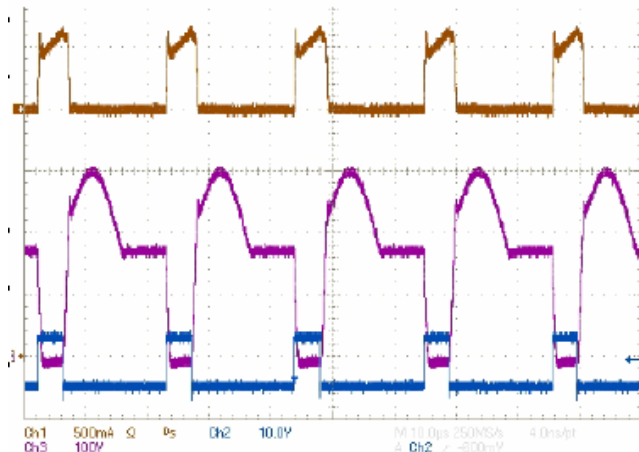


Fig. 8. Representative waveforms measured for the prototyped design shown in Fig. 7. $V_{IN} = 170$ VDC, $V_{OUT} = 24$ V, $f_s = 50$ kHz [3].

V. CONCLUSION

The gate driver design described here provides a generalized method for driving a normally on or quasi-off SiC JFET in a DC-DC converter. This circuit was designed to provide inherent safety as well as isolation from the main control circuit. An ideal application for this type of driver would be DC-DC converters that require gate driver isolation such as half- and full-bridge converters or single switch topologies that provide galvanic isolation between the input and output stages by means of a transformer (i.e. forward or flyback converter). A resonant reset forward converter was prototyped using this gate driver design and demonstrated the possibility of powering the controller on the secondary (or output) side of the power converter. This setup allows output voltage feedback circuitry to be directly coupled to the controller chip without the need of optocouplers for isolation purposes, which are parts known to be less reliable than magnetics. The flyback transformer of the gate drive circuit provides the necessary isolation between the main control signal and the driving voltage applied to the gate-source terminals of the main switching device. While satisfying these conditions, the gate driver presented here also proved to be a fast switching solution for an inherently safe gate driver design.

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