

# Optimized Gate Driver for Enhancement-mode SiC JFET

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## Abstract

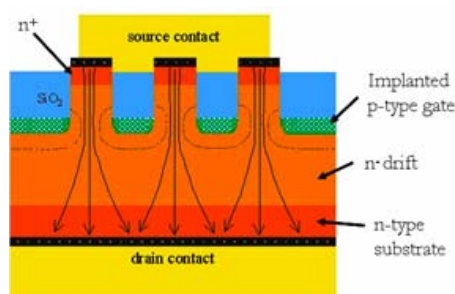
The first truly normally-OFF three-terminal SiC VJFET has been introduced and is being considered to replace MOSFETs and IGBTs in a variety of commercial applications. As the device's acceptance grows developers will be looking for optimized gate drive methods to achieve the best possible switching results to in turn yield higher system efficiencies. This paper provides a detailed investigation of the gate characteristics of the enhancement-mode SiC JFET and presents an optimal gate drive solution for driving the device in a half-bridge configuration. The importance of noise-immunity for the use of a reduced threshold-voltage device in the high- and low-side position of a bridge configuration will be addressed.

## 1. Introduction

Conventional wisdom that suggests SiC JFETs should only be normally-on devices has recently been superseded by the first commercially available pure enhancement-mode silicon carbide power JFET (EM SiC JFET). This new three-terminal, enhancement-mode device provides designers with a normally-off solution that maintains all the functionality and benefits of its normally-on counterpart. This new EM SiC JFET has a very small die size which requires very low gate-drive charge (25 nC gate charge). It is also affordable at higher volume than the SiC MOSFET because of the small physical size and other advantages device architectures. This compact EM SiC JFET is in single die form, without need for the dual die cascade assembly. It has no body diode and no gate oxide. A cross-

sectional illustration of the device structure is shown in Figure 1a, and a top view of a commercial TO-247 packaged 1200 V, 125 mOhm part is shown in Fig. 1b. From Fig. 1a, one can notice the simple device structure that is consistent with self-aligned manufacturing methods. The device is a typical vertical power device with a back-side drain contact, a top-side source, and recessed gate contacts. Unlike other well-known lateral channel normally on JFET structures [1], the channel is completely vertical between the recessed trench gate regions. This leads to a manufacturable process for the true normally off SiC JFET.

In this work we address effective use of the compressed threshold voltage of the EM SiC JFET. With a threshold voltage of ~1V, use of the EM SiC JFET in a bridge configuration must



(a)



(b)

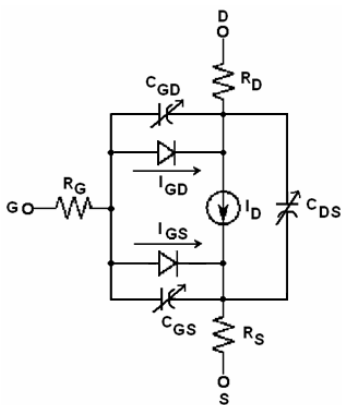
**Fig. 1:** SiC VJFET (a) cross-section and (b) TO-257 package.

be done properly to avoid the possibility of false triggering when the Miller capacitance of the alternate series switch is charged. The need for active/passive clamps or negative gate bias on the gate of each switch to prevent this possible problem is nothing new to power electronic designers using Si devices. Also, the use of low-threshold voltage MOSFETs in power electronic design has existed for years with specific design techniques and gate driver chips available for such devices. Concern for noise immunity with the low-threshold voltage EM SiC JFET in many applications can be addressed with one or more solutions presented in this paper. Also, a comparison between the device performance of the EM SiC JFET against commonly used IGBTs in applications with 480 VAC inputs as well as current PV inverters will also be presented. Lastly device performance in a half-bridge circuit, the building block for more advanced converter topologies, will be discussed.

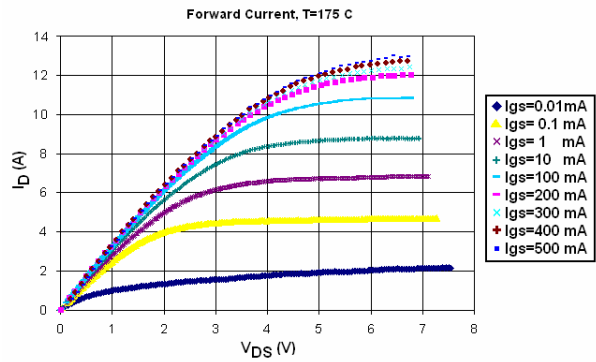
## 2. SiC Technology

### 2.1. Gate Structure and Requirements

It is important to first understand the effective circuit model of the EM SiC JFET before one can begin designing optimized power and gate control circuits specific to its use. Fig. 2 provides an equivalent schematic model of the vertical-channel SiC JFET. As shown, the gate-source junction exhibits a variable capacitance, much like a MOSFET, as well as a pn diode, much like a BJT. This presents two main requirements for the gate driver: delivery/removal of dynamic charge for charging/discharging the total gate capacitance and maintenance of the required steady state voltage/current



**Fig. 2:** Schematic representation of the SiC JFET



**Fig. 3:** Forward conduction vs. supplied DC gate current for  $T_j = 175^\circ\text{C}$

requirements of the gate-source diode. From the datasheet, a user can locate information for the required gate charge, approximately 25 nC for the 125 mΩ device, and I-V characteristics about the gate diode [2]. From Fig. 3 maximum forward conduction, at  $T_{J(\text{MAX})} = 175^\circ\text{C}$ , is achieved with DC gate currents of at least 100mA.

### 2.2. Device Losses

Semiconductor switches present two types of losses that affect the overall efficiency of a system; conduction losses and switching losses. Conduction losses are affected by the  $R_{\text{DS(ON)}}$  of the device during the conduction state while switching losses are dominated by the time it takes for a switch to transition between a fully blocking state to a conduction state and vice versa.

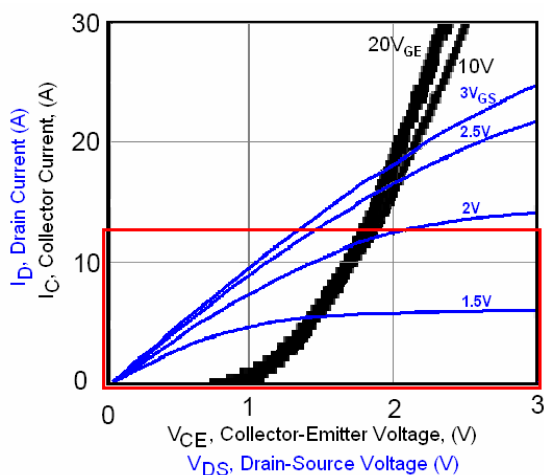
Fig 4 provides a comparison between the forward conduction characteristics of a 1200 V, 125 mΩ EM SiC JFET and the Fairchild FGL40N120AND Si IGBT commonly used in 480 VAC applications as well as current PV Inverters in the < 10 kW range. These particular applications typically demand a maximum drain current of ~10 A, which is an appropriate operating rating for the 125 mΩ EM SiC JFET. For these applications the IGBT is purposely oversized to manage the device losses by keeping the thermal resistance low. As shown in Fig. 4 the EM SiC JFET exhibits ohmic conduction characteristics that are similar to a MOSFET thus offering the opportunity to reduce the conduction losses of the system significantly.

The switching behavior of the EM SiC JFET is much like that of a MOSFET as it is also a unipolar device. However, since the EM SiC JFET has much lower intrinsic capacitances than

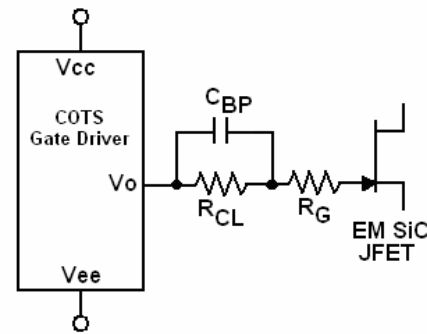
a comparable MOSFET it has the ability to switch on and off extremely fast. The switching losses are evaluated in a standard double-pulsed, diode-clamped, inductive load circuit. Both the 125 mΩ EM SiC JFET and the FGL40N120AND IGBT were evaluated for switching energy using the same test fixture. Table 1 provides a comparison between the switching energy losses of each device at both room temperature and 150°C. Recommended gate drive conditions specified by the manufacturer were used for driving the IGBT in the test circuit.

### 3. Gate Drive Design

The transition speed is ultimately limited by the device; however, the performance of the gate driver can impact this speed considerably. The main function of the gate driver is to deliver/remove the necessary gate charge required by the internal gate-source and miller capacitance of the device in order for the device to transition between states. The faster the gate driver can perform this task, the faster the device will transition. Therefore it is important to use a properly designed gate driver circuit for maximum performance of the device within a practical system application. Because of the absence of a body diode in the vertical-channel EM SiC JFET, the basic limitation on device performance is the peak dynamic current that can be supplied by the gate drive. But there are other system concerns arising from the effects of very large  $dV/dt$  on the rest of the system that might impose lower limits.



**Fig. 4:** Forward conduction comparison between the 125mOhm EM SiC JFET and FGL40N120AND IGBT



**Fig. 5:** AC coupled gate drive for drop-in replacement

#### 3.1. AC Coupled Driver

Prior work has documented the use of the EM SiC JFET as a drop in replacement for MOSFET/IGBT's in switch-mode applications like an active PFC and a solar inverter [3],[4]. In both applications the gate drive scheme was an AC coupled drive that mimics a BJT driver. In these references, a paralleled RC network was connected between the gate terminal and the output of the driver IC (Fig. 5). This particular gate driver may not be the most optimal solution for achieving the best possible switching speeds, but it is otherwise an effective, simple, and cost effective driver technique for immediate evaluation of the EM SiC JFET in current applications. The gate resistor is used to set the DC operating point in the "on" state by dropping the potential difference between the high level output of the driver IC and the required gate-source voltage of the EM SiC JFET at  $I_{GFWD}$ . The bypass capacitor is used to rapidly deliver/remove the required gate charge for a fast turn-on and turn-off. MOSFET and IGBT users are accustomed to interfacing the Si devices to a driver IC through a gate resistor. For immediate evaluation of the EM SiC JFET it is recommended that the Si device be replaced with the SiC device, the gate resistor value be changed to that required by the SiC EM JFET, followed by the installation of a bypass capacitor connected in parallel with the gate resistor. Recommendations for sizing each component and example switching waveforms can be found at the end of the device datasheet [2].

While the AC coupled driver is an effective means of driving the EM SiC JFET and can achieve impressively low switching loss numbers, it is not the optimal driver for all ranges of duty factors and switching frequency. To consistently obtain the fastest switching performance

possible it is necessary for the bypass capacitor of the RC network to be fully discharged prior to the next switching event. The size of this capacitor depends on the specifics of the application and the driver IC. Any particular value may need more time to discharge than that available for certain combinations of switching frequency and duty factor. While no operational problems will result from not fully discharging this capacitor; slower turn-on transitions may result as there is less stored charge for driving the gate capacitance at the next turn-on event. Therefore additional DC-coupled gate driver designs that can operate over a wider range of switching frequencies and duty factors are necessary.

### 3.2. Optimized Drivers

High frequency applications need a driver that is not dependent on an RC time constant for best performance. A two stage, DC coupled driver design has been developed specifically for the JFET (see Fig. 6). This circuit accepts a single PWM control signal and generates a second PWM signal that is  $\leq 15\%$  the pulse width and synchronized with the original control signal. The generated pulse drives MOSFET M1 which provides a high peak current source for quickly charging the device's gate and miller capacitance at turn-on. The original control pulse is applied to the gate of MOSFET M2 that will supply the necessary steady state DC gate current required to maintain conduction. Current limiting resistor R1 is properly sized to set the forward gate current  $I_{GFWD}$  while stepping down the voltage from the positive rail voltage to that required by the gate of the JFET. R1 is sized with the same approach used for the gate resistor in the AC coupled RC drive circuit. The complement of

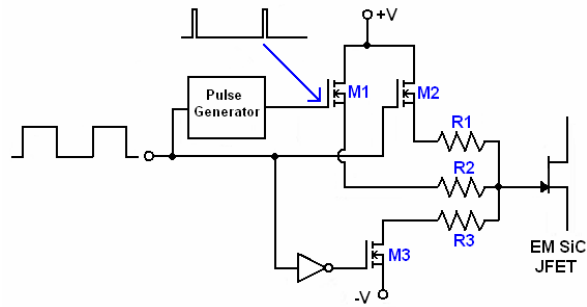


Fig. 6: Two stage gate driver for EM SiC JFET

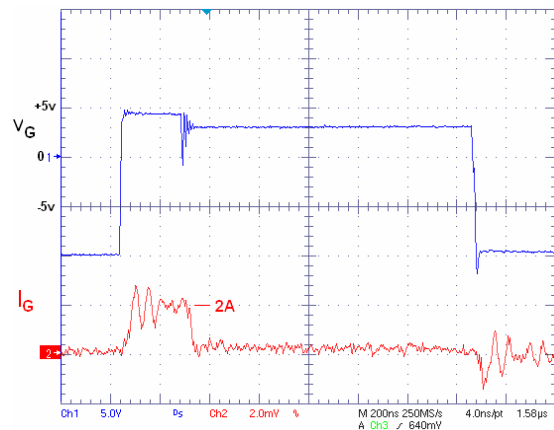


Fig. 7: Gate waveforms produced by the two stage driver

the user supplied PWM pulse is formed by an inverter and applied to the gate of a third MOSFET, M3. When the PWM signal goes low, M3 turns on pulling the JFET gate low through a  $1\ \Omega$  pull-down resistor R3. An oscilloscope image of the gate waveforms produced by the two stage driver are shown in Fig. 8. Switching energy measurements were conducted using the two-stage, DC-coupled driver (see Fig. 8). The visible noise on the gate current waveform is a result of using a Rogowski coil at its lower limits.

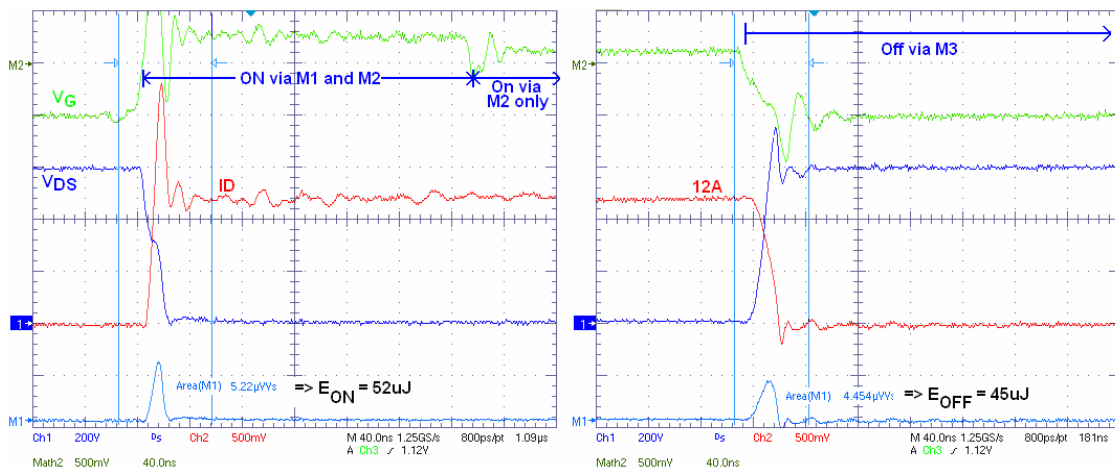


Fig. 8: Switching Energy Waveforms using the two stage driver

**Table 1.** Energy Loss Comparison. Clamped inductive load circuit VDC = 600V, IL = 12A.

Device	Driver Circuit	Eon (uJ)	Eoff (uJ)	Eon+Eoff (uJ)
125 mΩ SiC JFET	AC coupled	57	35	92
125 mΩ SiC JFET	DC Coupled	52	45	97
FGL40N120AND	DC Coupled	174	381	555

The resulting switching losses for the 125 mΩ EM SiC JFET driven by each of the two types of driver circuits discussed here are compared in Table 1. As shown, both types of drives produce similar fast switching results; however, the two stage DC coupled drive is not limited by switching frequency or duty factor. The results were also compared to the leading IGBT technology commonly used in 480 VAC applications and solar inverters with power ranges < 10 kW. No MOSFET device was considered because there is no MOSFET technology available with voltage ratings suitable for a 480 VAC (700 V DC) application. Based on the information provided in Table 1 and Fig. 4 a significant improvement in system efficiency can be realized with only a change in semiconductor switches.

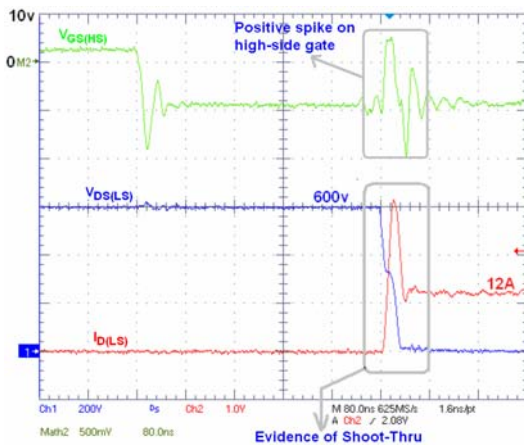
#### 4. Performance in a Half-Bridge

The low threshold-voltage of the EM SiC JFET could increase the susceptibility of the device to uncontrolled switching when, for example, the device is in a half-bridge configuration. The EM SiC JFET is subject to the same “Miller effect” problems that occur with MOSFETs and IGBTs. Like MOSFET/IGBTs, the possibility of the gate-source voltage being pulled positive for a short duration can cause a shoot-thru event if not properly prevented. Maintaining the gate of the blocking switch at a negative voltage is recommended to increase the available sink current into the gate drive and to increase the margin between threshold and the transient gate potential produced by dV/dt driven displacement current during half-bridge switching events. Since the EM SiC JFET is normally-off, blocking full rated voltage at  $V_{GS}=0$  V, this negative rail can be derived dynamically once normal converter operation begins.

Similar to MOSFETs and IGBTs there are three common approaches for preventing this positive spike in gate voltage from reaching the device’s threshold voltage. A first approach is typically increasing the voltage differential between the

turn-off voltage and the threshold by adding or increasing the amount of negative voltage. This is an easy solution and does not impact the switching performance of either the high- or low-side device. As with all field-controlled power devices there is a limit to the amount of negative voltage that can be applied to the gate of the EM SiC JFET. The device datasheet limits the negative voltage to -15V, therefore if a positive gate spike is still evident after -15V another approach must be taken. The second option for preventing a positive spike on the blocking device is by adding a capacitive clamp across the gate-source terminals of the blocking device. By including the additional capacitance very close to the gate-source terminals, the voltage rise due to the displacement current through the Miller capacitance can be reduced further. This will require the gate driver to deliver more gate charge to the device during its turn-on switching event resulting in a modest increase in gate drive power and possibly a slightly slower turn-on speed. The last option is a downward adjustment of the dV/dt by adjusting the series gate resistance  $R_G$  of the AC coupled drive or  $R_2$  of the two-stage driver. This will reduce the peak current through the Miller capacitance of both switches and reduce the probability of shoot-through through the blocking switch. This third option will obviously result in slower switching than the maximum possible.

Fig. 9 and Fig. 10 provides oscilloscope waveforms measured across the EM SiC JFETs of a phase leg of a half-bridge converter. Fig. 10 shows  $V_{GS}$  for the high-side device with no preventative measures taken to avoid shoot-thru caused by the “miller effect” during the turn-on event of the low-side switch. For this application it was undesirable to adjust the negative rail beyond -10 V and thus a capacitive clamp was used to eliminate this positive spike on the high-side gate voltage. Fig. 11 provides waveforms after a 10 nF capacitive clamp was connected across the gate-source of the high-side device. As shown the positive spike on the gate voltage, as well low-side drain current spike, were much reduced with the addition of the



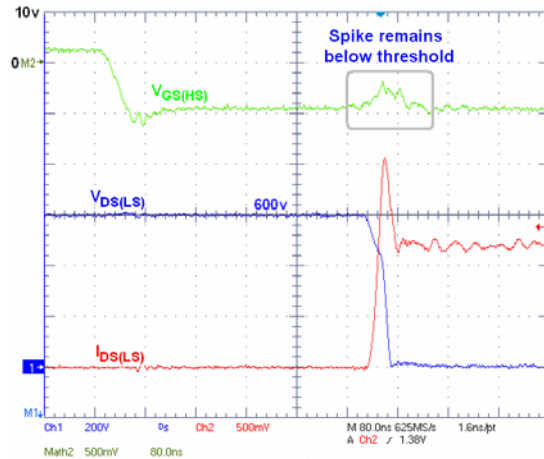
**Fig. 9:** Switching waveforms for high and low-side JFETs in a half-bridge.  $V_{GS}$  of high-side device = top waveform,  $V_{DS}$  and  $I_D$  of low-side device = lower waveforms.

capacitive clamp. The remaining transient current through the low-side switch in Fig. 11 is the normal displacement current required to charge the high-side (blocking) switch and anti-parallel rectifier to the 600-V bus voltage.

## 5. Conclusion

The new EM SiC JFET is an ideal candidate for the replacement of MOSFETs and IGBTs in both high-side and low-side switching applications. Simple modifications to standard driver techniques currently used for MOSFETs and IGBTs produces an AC coupled drive that has proven to be an effective drive solution for initial evaluation of the EM SiC JFET in most switching applications. However, there exists frequency and duty factor limitations for the AC coupled drive that can be best overcome with a DC-coupled gate drive. A two stage, DC coupled drive was developed based on the specific needs of the EM SiC JFET that also produced very low switching losses. Both types of drive produce similar switching losses but the DC-coupled drive is more complex in that it requires more components than the AC-coupled drive. Thus the needs of the application will dictate the optimal choice.

Using either approach it is evident that total system efficiency can be increased by using the EM SiC JFET in place of IGBTs in high voltage applications due to the much lower switching and conduction losses. Also proper application of a negative voltage rail can eliminate potential



**Fig. 10:** Switching waveforms for high- and low-side JFETs after 10 nF capacitive clamp was added.  $V_{GS}$  of high-side device = top waveform,  $V_{DS}$  and  $I_D$  of low-side device = lower waveforms.

noise immunity problems resulting from the reduced threshold voltage of the device.

## 6. References

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