

# Inherently Safe DC/DC Converter Using a Normally-On SiC JFET

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**Abstract** - This paper examines the design of an inherently safe DC-DC converter specifically for normally on silicon-carbide based power JFETs. The converter is targeted for ambient temperatures of 225°C. A demonstration converter board has been completed and tested illustrating proof of principle of the self-biased gate driver configuration for deriving a stable 5-V dc output from a 25-V dc input. The converter has also demonstrated conventional “off-line” 120 VAC operation to develop a 12 V dc output.

## I. INTRODUCTION

As silicon carbide device technology continues to mature [1], SiC applications are being introduced to address new requirements. Diverse industries ranging from oil exploration to automobiles have new requirements for higher ambient temperature operation. Operation at 225°C ambient temperature is a standard application addressable by SiC power devices. The most mature SiC based power device besides the Schottky rectifier is the junction field effect transistor (JFET). The threshold voltage for the SiC JFET can range from quite negative (normally on) to slightly negative (quasi-on) to slightly positive (normally off) [2]. The use of pure normally on power devices in conventional switch mode converters is a concern during start up or abnormal operation of the gate driver because of the possibility that the dc input bus will be overloaded and the switch damaged from overheating. Since normally off SiC JFETs sacrifice low device on resistance for this attribute, inherently safe circuits that use normally on parts are a better choice. In this work, a buck converter is described that is inherently safe. In fact, a normally-on SiC JFET is required for the converter to self-start. The SiC JFET used in this work is a 600-V blocking device that has extremely low internal gate resistance, and thus address the gate resistance problem reported in previous work [3].

## II. CIRCUIT OPERATION

To provide an overview, the buck converter operation is briefly explained. The switching cycle begins when the transistor, shown in Fig. 1, is switched on by the controller. As illustrated in Fig. 2, during the  $t_{on}$  period the inductor current will increase linearly. During this time the input source delivers energy directly to the load, while the buck inductor begins to store the energy necessary to power the load during the time that the transistor is turned off. Once the required energy is stored within the core of the inductor, the transistor

is switched off. This causes the inductor voltage to reverse, or flyback, which drives the Schottky diode (SBD) into conduction, thus commuting the current to the SBD that was flowing through the transistor. During the  $t_{off}$  time shown in Fig. 2 the buck inductor delivers stored energy to the load. As the amount of stored energy decreases, the magnitude of the inductor current also decreases. Assuming that the inductor current is non-zero at the beginning of the switching cycle (i.e., *continuous conduction mode*), then the ratio of the output voltage to the input voltage is determined by the duty ratio  $D = t_{on}/T$ , where  $t_{on}$  is the period of conduction of the switch and  $T$  is the period of the switching cycle. In an ideal buck converter operating in continuous conduction mode the product of the duty ratio and the input voltage determines the output voltage of the converter, i.e.,  $V_{out} = DV_{in}$ . In a practical buck converter, series resistance in the transistor and inductor will cause the output voltage to drop as the converter is loaded. The controller can compensate voltage droop by increasing the duty ratio.

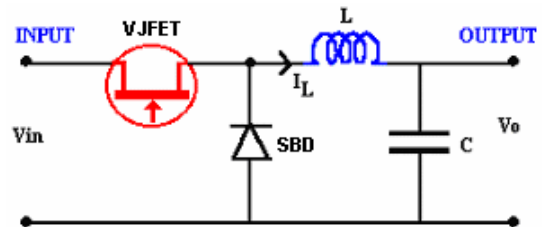


Figure 1. Simplified buck converter circuit diagram.

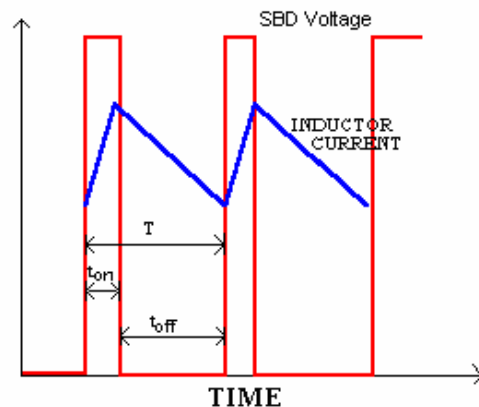
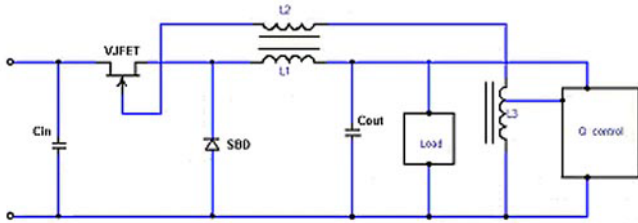


Figure 2. Typical waveforms for a buck converter in continuous conduction mode.

Before determining the size of the buck inductor for the circuit, it is necessary to specify an operating mode. The choice of continuous conduction mode proved to be the most favorable for achieving good efficiency since it was necessary that the current ripple through the buck inductor, defined as the ratio of the ripple current to the average current  $\Delta I_{Lpk}/I_{AVE}$ , be as small as possible. Other benefits of a low  $\Delta I_{Lpk}/I_{AVE}$  are that the size of the wire necessary for the transformer is minimized, and copper losses in the transformer due to the skin effect are reduced [4].

As with any power converter that uses a field controlled switch, a gate driver is required to operate the switch; and with a normally on device comes the concern about gate driver failure. Since a normally on device is effectively conducting at zero gate bias, the input of the buck converter is directly connected to the output at start-up. The JFET must pinch off before the output sees the input voltage, as any overshoot could be harmful. While driving a SiC JFET is similar to driving a MOSFET, there are differences. Each is a voltage-controlled device, but the high and low logic levels required to turn each of the devices on and off are much different. An n-channel enhancement-mode MOSFET is a normally off device that requires a gate voltage of less than the threshold value (0 V will do) for turn off, and up to +20 V for turn on. The SemiSouth SiC HEL<sup>2</sup>FET™ used in this work is a normally on device that requires a gate voltage of -5 V for turn off and a slightly positive gate voltage of +2 to +3 V to obtain the maximum  $I_{DSS}$  rating.



**Figure 3.** Practical buck converter made with a HEL<sup>2</sup>FET™ and a SemiSouth SiC SBD.

A practical circuit design is shown in Fig. 3 that requires an autotransformer, L3, to accept the control pulse at a winding tap to generate the positive gate voltage necessary to turn the HEL<sup>2</sup>FET™ on. A secondary winding, L2, is added to the buck inductor, L1. If L2 has the same number of windings as L1, then the gate terminal will float to the same buck inductor potential as the source terminal, thus eliminating the need for a floating ground reference for the gate control circuitry. The required control voltage is determined by a loop equation that includes the gate and source terminals and the output:

$$-V_{OUT} - V_{L1} - V_{GS} + V_{L2} + V_P = 0. \quad (1)$$

This simplifies to:

$$V_{GS} = -V_{OUT} + V_P, \quad (2)$$

where  $V_{OUT}$  is the output voltage,  $V_{L1}$  is the voltage developed across the buck inductor,  $V_{L2}$  ( $= V_{L1}$ ) is the voltage across the coupled winding,  $V_{GS}$  is the gate-source voltage on the HEL<sup>2</sup>FET™, and  $V_P$  is the voltage developed across the secondary of the autotransformer. Equation (2) results from the simplification of (1) when the coupled inductor has the same number of turns as the buck inductor, ensuring that the voltages across each cancel.

While  $V_P$  is zero,  $V_{GS}$  is held at the negative value of the output voltage. Therefore,  $V_P$  develops the positive voltage required to switch the HEL<sup>2</sup>FET™ to its minimum on resistance. The autotransformer is wound so that when a voltage  $V_Q$  is applied across the primary, a voltage  $V_P$  is developed across the secondary:

$$V_P = aV_Q, \quad (3)$$

where  $a$  is the turns ratio of the autotransformer. Since the controller is self-powered by means of the output voltage, the logic high value of the output voltage pulse  $V_Q$  is approximately equal to the output voltage. Letting  $V_Q = V_{OUT}$  the required  $a$  for a desired  $V_{GS}$  value is

$$V_{GS} = -V_{OUT} + aV_Q$$

$$a = \frac{V_{GS} + V_{OUT}}{V_{OUT}}. \quad (4)$$

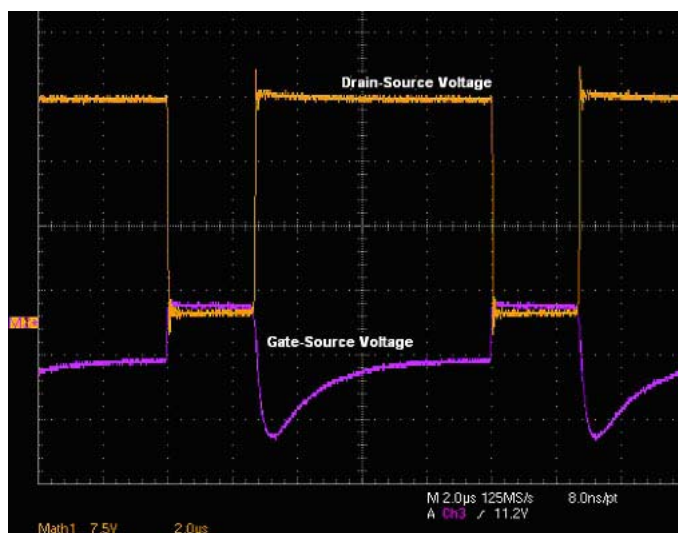
The HEL<sup>2</sup>FET™ used in this design delivers maximum  $I_{DSS}$  at  $V_{GS} = +3$  V. The turns ratio of the autotransformer was determined from Eq. (4) to be 1.6.

When the controller output is low,  $V_Q = 0$  and  $V_{GS} = -V_{OUT}$ . Provided that  $V_{OUT}$  exceeds the magnitude of the pinch off voltage of the JFET (a design requirement), the JFET must turn off. The JFET current is limited to  $I_{DSS}$  at any  $V_{GS}$ . During start up, the charging of the output capacitor is controlled by the JFET until it charges to the pinch-off voltage; resulting in controlled start up without overshooting the maximum safe output voltage. If the controller fails to operate, the converter output voltage reaches a quiescent value that is limited by the pinch off of the JFET.

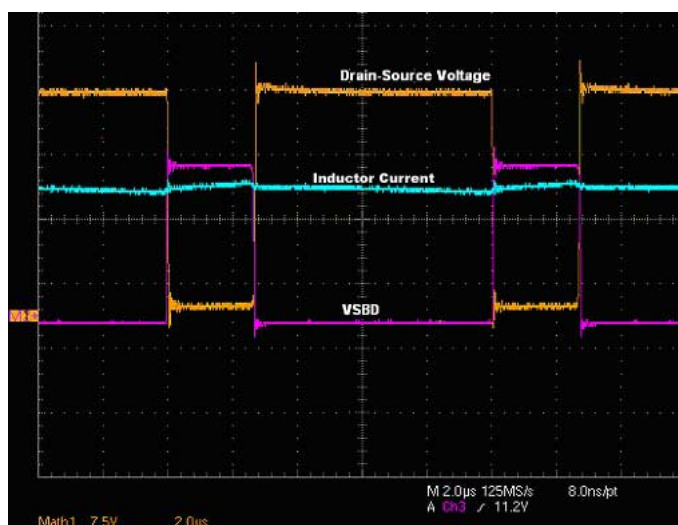
### III. TEST RESULTS

After fabricating a demonstrator circuit based on the design process described the following test results were obtained. For nominal load, the quantities listed in Table I in Appendix A were measured. This table lists the room temperature results for the converter running with a “Generation 2,” ultra low gate resistance vertical-trench JFET [1]. The following switching waveforms were captured for the Generation 2 part in order to illustrate the ideal switching behavior observed

with the prototyped design. In Fig. 4, the gate-source and drain-source voltages of the HEL<sup>2</sup>FET™ were measured. As the gate voltage approaches its maximum positive value of 3 V the transistor quickly begins to conduct allowing the drain-source voltage to drop to a voltage less than 2 V. Once the control pulse goes low, the gate-source voltage quickly flies back to the reset voltage of the autotransformer, providing additional negative bias to assist in rapidly turning off the HEL<sup>2</sup>FET™. The autotransformer is reset by means of a parallel resistor, and  $V_{GS}$  eventually returns to  $-V_{OUT}$  plus the SBD forward voltage drop. During both turn on and turn off, the gate driver does not limit the available gate charge to the gate-drain diode; this is determined by the internal gate resistance of the VJFET itself.



**Figure 4.** Oscilloscope traces of  $V_{DS}$  and  $V_{GS}$ .



**Figure 5.** Oscilloscope traces of the buck inductor current,  $V_{DS}$  and  $V_{SBD}$  (measured with reference to the anode).

Figure 5 displays the drain-source voltage, the voltage across the Schottky barrier diode (SBD), and the low-ripple buck

inductor current. The current waveform illustrates that commutation between the transistor and the free-wheeling diode (which occurs at the peak value of the current) is fast and efficient, owing both to the speed of the HEL<sup>2</sup>FET™ and to the negligible reverse recovery of the SiC SBD.

These factors resulted in small dynamic losses in the transistor despite the high switching frequency, which was reflected in the modest case temperature rise of about 20°C (free air convective cooling). With such a low transistor temperature rise the converter could be operated at the maximum specified ambient temperature of 250°C without exceeding the HEL<sup>2</sup>FET™ 300°C junction temperature rating.

The prototype was designed to demonstrate a low power, high ambient temperature voltage regulator. Detailed results are found in Appendix A for room temperature and high temperature operation of the switch. At room temperature, the measured efficiency was 84%. Two-thirds of the measured losses were in the semiconductor devices themselves. Of this the SBD contributed ten times as much power loss as the JFET for the simple reason that the SBD cut-on voltage represents a fixed loss; and given the relatively low output voltage and the low duty factor of the circuit (the conduction time for the SBD is 77% of the total switching period) this fixed loss is significant. Since the SBD has a negligible reverse recovery transient, all losses associated with the SBD are conduction losses. Eliminating the SBD conduction loss would increase the converter efficiency to 95%. Synchronous rectification, while not implemented here, would permit the higher efficiency. However, high temperature operation, not efficiency, is the application driver.

High temperature measurements were conducted for a case temperature of 225°C by externally heating the JFET (all other components were not externally heated). Increasing the case temperature of the JFET produced a 20% drop in efficiency. This is due solely to the fact that the JFET immediately available for use in the demo circuit was underrated in current. As with any unipolar device, the JFET  $I_{DSS}$  rating decreases as temperature increases. The test results at the higher case temperature reflect the fact that the saturated drain current of the JFET dropped below the average current rating needed to deliver the full rated power to the load with comparable efficiency as the room temperature tests. Otherwise, the demo circuit operation was equivalent to the test with lower case temperature. The efficiency at high temperature can be increased by selecting a JFET with a higher current rating. A transistor with an  $I_{DSS}$  rating at maximum junction temperature slightly above the specified average output current of the buck converter demands about a factor of 2.5 higher current rating than the device used in this demo, which is now available from current production.

The circuit design reported is self starting, since at initial start-up the normally on JFET allows current to flow charging the output capacitance. As the output capacitor charges, the JFET

gate source junction is increasingly reverse biased, which begins to pinch off the transistor. Provided that the minimum turn on voltage of the controller is reached before the JFET fully pinches off (an easily achieved design requirement), the controller begins to oscillate and to generate the desired control pulse necessary for full-scale operation. This circuit is both self starting and inherently safe because if the controller were to fail, the output capacitor would hold  $V_{GS}$  at  $-V_{OUT}$ , which would pinch off the transistor and separate the input from the output.

Additionally, “off line” operation of the circuit with the same transistor has been demonstrated with a 120 V RMS ac input voltage. While blocking a peak voltage of 166 V, the converter delivered 12 V dc at 77% efficiency. Otherwise, the same self-powering, self-starting, and inherently safe operation was observed.

#### IV. CONCLUSION

The fabricated prototype demonstrated representative buck converter operation while proving to be self-starting and inherently safe. The power loss analysis revealed that the Generation 2 SiC JFET had decreased switching losses and faster switching times made possible by the reduction of internal gate resistance. By introducing a synchronous rectifier to reduce the conduction loss in the free wheeling rectifier and increasing the current rating of the power switch, the overall efficiency of the design would increase to 95% at an ambient temperature of the power switching components of 225°C.

#### V. REFERENCES

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## APPENDIX A

**Table I. Room Temperature and High Temperature Test**

			Room Temperature Test (5 W @ 23°C)	High Temperature Test (5 W @ 225°C)
<b>1. Input</b>				
	Input Voltage	$V_{IN}$	25 V	25 V
	Input Current	$I_{IN}$	0.25 A	0.28 A
	Input Power	$P_{IN}$	6.25 W	7 W
<b>2. Output</b>				
	Output Voltage	$V_{OUT}$	5.12 V	5.25 V
	Output Current	$I_{OUT}$	1.021 A	0.855 A
	Output Power	$P_{OUT}$	5.23 W	4.48 W
	Efficiency	$\eta$	84 %	64 %
<b>3. Switching Period</b>				
	Rise time (VJFET)	$t_r$	18.4 ns	n/a
	Fall time (VJFET)	$t_f$	30.4 ns	n/a
	Conduction Time (VJFET)	$t_{on}$	2.52us	2.68us
	Switching Period	$T$	9.92us	10.0us
	Switching Frequency	$f_s$	100kHz	100kHz
	Duty Factor	$D$	0.23	0.268
<b>4. Temperature*</b>				
	Ambient	$T_A$	23.0°C	23.0°C
	Case	$T_C$	34.0°C	225°C
<b>5. Power Loss</b>				
	Loss during turn on transient of JFET	$\langle P_{FETrise} \rangle$	0.0116 W	n/a
	Loss during conduction period of JFET	$\langle P_{FETon} \rangle$	0.0081 W	n/a
	Loss during turn off transient of JFET	$\langle P_{FETfall} \rangle$	0.0378 W	n/a
	Total power loss for JFET	$\langle P_{FET} \rangle$	0.0575 W	n/a
	Loss during conduction period of SBD	$\langle P_{SBDon} \rangle$	0.724W	n/a
	Total power loss for semiconductor devices	$\langle P_{SEMI} \rangle$	0.782W	n/a
	Total power loss for other components**	$\langle P_{other} \rangle$	0.238 W	n/a

\* A 6-finger free air/standing heat sink was attached to the back of the TO-257 packaged VJFET with a screw. An RTD was also screw attached to measure case temperature.

\*\* ‘Other components’ include passive components, control circuit, and copper traces on PCB.