High-Temperature Reliability Assessment of 4H-SiC Vertical-Channel JFET Including Forward Bias Stress

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Abstract. In this work, we report the most recent reliability results of the 1200-V SiC vertical-channel JFETs (VJFETs) under reverse and forward bias of the gate-source diode at temperatures up to 200 °C. The preliminary results indicate that continuous forward bias stress of the gate-source diode at 200 °C for 112 hours produced no observable change in the forward conduction or transient or reverse blocking characteristics of the vertical-channel JFET. This preliminary result suggests that devices based on this structure, such as the enhancement-mode (normally off) SiC VJFET, may not be effected by the recombination enhanced defect creation process and the associated increase in on-resistance, related to body-diode conduction in the SiC DMOSFET and the SiC lateral-channel depletion-mode JFET. Since the vertical-channel JFET has no body diode, no degradation is possible from the reverse conduction mode of operation.

Introduction

The maturation of SiC power devices for power-electronics applications is leading to the need to assess the reliability of these devices, especially under conditions expected from their use in applications. One such condition is bipolar conduction in otherwise unipolar devices. The risk of bipolar conduction in SiC is the activation of degradation caused by stacking-fault formation in the device volume where electron-hole pair recombination takes place. Pure unipolar operation of a MOSFET or a JFET does not cause such degradation, but reverse conduction through the built-in p-n junction "body diode" of the SiC MOSFET has been demonstrated to cause degradation in the unipolar forward-conduction characteristics as observed by an increase in the MOSFET on-resistance [1]. This reliability problem affecting long-term stability has been reported in lateral-channel JFETs as well [2]. The conclusion is that any unipolar device with a body diode that conducts significant "reverse" current when the p-n junction is under forward bias is susceptible to degradation of the unipolar terminal characteristics due to stacking fault creation in the drift region. However, as shown in Fig. 1, there are at least two fundamental ways to make a JFET. In Fig. 1(a), the typical lateral-channel JFET is shown. This device has a body diode. In Fig. 1(b), the typical vertical-channel JFET is shown. This device does not have a body diode. Instead, only a gate-drain diode and a gate-source diode are observable from the terminals of the device. During normal operation in applications, the gate-drain diode of the vertical channel device will not become forward biased and therefore forward bias degradation can be excluded. However, forward biasing the gate-source diode is a normal operating mode, especially for the

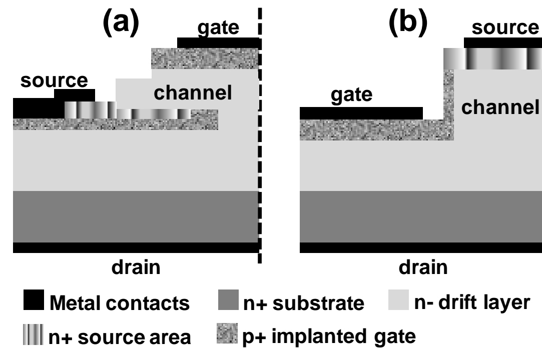

Fig. 1 Schematic cross sections of half cells for two different power JFETs structures:
a) LV-JFET with both lateral "pre-channel" and vertical channel
b) VJFET with only the vertical channel

enhancement-mode (normally off) devices now being reported [3]. In this work, we report the most recent assessment of high-temperature reliability of the 3.8 mm^2 1200-V normally-on SiC VJFETs under different bias conditions at temperatures up to 200 °C, including a recent preliminary study examining the hypothesis that forward biasing the gate-source diode of such JFETs might produce degradation. At high temperatures, these devices were designed to fully block 1200 V at V_{GS}=-15 V.

Experimental

The 1200-V 4H-SiC VJFET structure is shown in Fig. 1(b). Upon completion of the device fabrication, twelve 1200-V 4H-SiC VJFETs selected randomly from five wafers (W1 to W5) were assembled separately in TO257 packages and sealed with a commercially available dielectric-gel to passivate and encapsulate the device at full working voltage. Average on-resistance of these devices is 0.11 Ω at V_{DS} = 1 V and V_{GS} = 2.5 V with a standard deviation of 1.3% at room temperature (RT). DC characteristics of all the devices were pre-measured before any electrical and thermal stresses were applied. Afterwards the devices received the electrical stresses first under reverse bias at RT and 200 °C and then forward-bias at 200 °C in an oven.

Results and Discussion

Reverse Bias Stress Test. To investigate off-state stability of the SiC VJFETs with temperature variations, all twelve devices were continuously reverse-biased at V_{DS} = 900 V and V_{GS} = -10 V through two temperature cycles between RT (T1) and 200 °C (T2) in an oven for a total of 194 hours. At the beginning of the test, the devices were reverse-biased at RT for a couple of hours to stabilize the leakage current. Then the HTRB (high-temperature reverse bias) system ramped the temperature from RT up to 200 °C in 30 minutes and stayed at 200 °C for 24 hours. The heater was then turned off so that the HTRB system cooled to RT without removing the reverse bias stress from the devices. After the reverse biased devices remained at RT for over 15 hours, the temperature of the HTRB system was again brought up to 200 °C and the devices were soaked for over 110 hours at 200 °C before the heater was once again turned off and the system cooled back to RT. Both the total and the individual drain leakage currents (I_D) were monitored throughout the reverse-bias test period.

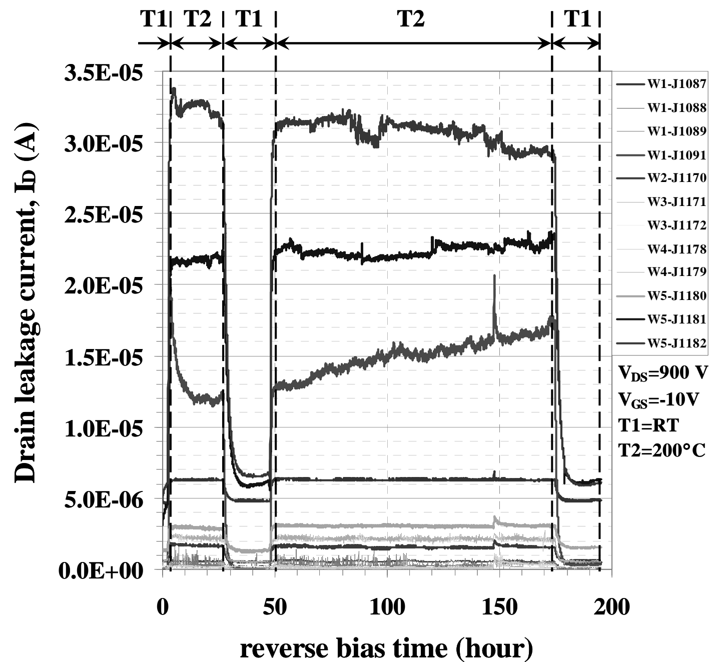

Fig. 2 Drain leakage current of twelve SiC VJFETs at V_{DS}=900 V and V_{GS}=-10V for two temperature cycles between RT to 200 °C for 194 hours.

As shown in Fig. 2, the drain leakage current of all devices at 200 °C are very low with a maximum leakage current density of less than 9 μA/mm^2 for any one device. Differences in the drain leakage current among these 12 devices could be due to process variations from wafer to wafer. Also shown in Fig. 2, the drain leakage current of all tested devices has a monotonic dependence on temperature and stabilizes at the final temperature with insignificant changes. Unlike the temperature-dependent forward conduction of the SiC VJFET caused by the normal reduction of electron mobility at high temperatures,

the reverse leakage current density is often dominated by the leakage at the periphery of the SiC device. Leakage at the periphery is influenced by such factors as the design of the edge termination and the quality of the surface passivation. Assuming that the devices are free of physical defects, what we observe in Fig. 2 indicates that the leakage current density is temperature dependent (increasing with temperature) and rapidly reaches a thermally stable level under the above reverse bias condition at the final temperatures.

Forward Bias Stress Test. To provide an initial assessment of reliability for the SiC VJFETs under forward bias at high temperature and to examine the hypothesis that forward biasing the gate-source diode of the SiC VJFET might produce conduction degradation due to injection of minority carriers from the p-type gate into the n-type drift layer, a forward bias stress test (FBST) was conducted on one device (W5-J1182) at V_{GS} = 2.5 V and 200 °C for 112 hours. In order to minimize the junction power dissipation, the drain current, I_D, was set to 1 mA during the FBST so that the gate p-n junction and case temperatures can be assumed to be approximately the same. Several parameters were monitored and recorded at a sample rate of one scan per minute through the entire test. The parameters were the drain voltage (V_D) at the applied drain current and gate bias, the corresponding forward gate-source current (I_{GS}), and the case and oven temperatures. As shown in Fig. 3, slight variations in I_D were due to the power supply used in this test, which is very sensitive to the ambient temperature fluctuation at such low I_D level. Despite the small variability of I_D, no significant change in the forward voltage drop (V_D) was observed during the FBST at 200 °C, indicating that forward biasing the gate-source diode over the period of the test did not produce degradation of the forward conductivity in the channel or the drift region. To confirm the above observation, the device was re-characterized after the FBST in order to compare with its pre-FBST characteristics. As shown in Fig. 4, the forward conduction, transient, and reverse blocking characteristics of the device W5-J1182 remained virtually unchanged after the FBST at 200 °C for 112 hours.

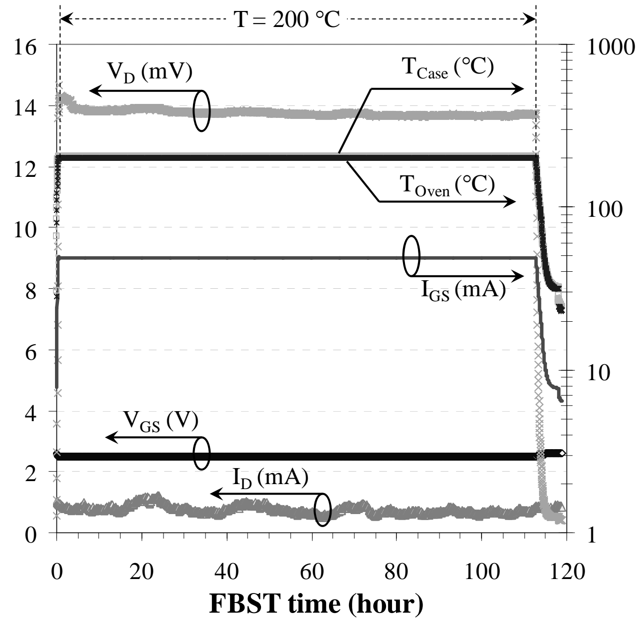

Fig. 3 Drain voltage (V_D) at the applied drain current (I_D) and gate bias (V_{GS}), the corresponding forward gate-source current (I_{GS}), and case and oven temperatures vs. FBST time of device W5-J1182.

As reported by many groups [1, 4, 5], the reason for degradation of the SiC bipolar power devices under forward bias is the formation of stacking faults in the drift layer due to electron-hole recombination induced by injection of the minority carriers across a p-n junction. Because the energy released from electron-hole recombination exceeds the threshold energy required to form or expand the stacking fault, increasing the p-n junction forward current density will enhance formation of the stacking fault. In practice, observing a significant rate of degradation of the forward conductivity requires the bipolar current density to exceed a threshold. In this work, since even at 200°C the forward gate current is no more than 50 mA at V_{GS} = 2.5 V as seen in Fig. 3, a negative result is not surprising because the low current density (1.4 A/cm^2) is about the same as the minimum thresholds reported to cause a significant rate of stacking fault formation [5]. These results suggest a negative result for the hypothesis that the forward conductivity of the SiC VJFET will degrade due to forward-bias conduction across the gate-source p-n junction under practical operating conditions.

Summary

In summary, the preliminary results on high-temperature reliability assessment of the 4H-SiC VJFETs indicate obvious mechanisms to suggest concern that irreversible degradation due to electron-hole recombination-induced stacking fault defects will arise through the practice of forward biasing the VJFET to turn-on the enhancement-mode VJFET and to enhance the on-state conduction of the depletion-mode VJFET. Off-state reliability of the SiC VJFETs through two temperature cycles between RT and 200 °C was found to be excellent. Testing will continue on more devices under the FBST conditions described in this work to build confidence in the tentative conclusion that forward-conductivity degradation is unlikely to be a problem for these vertical-channel SiC JFETs under normal operating conditions at temperatures up to at least 200 °C.

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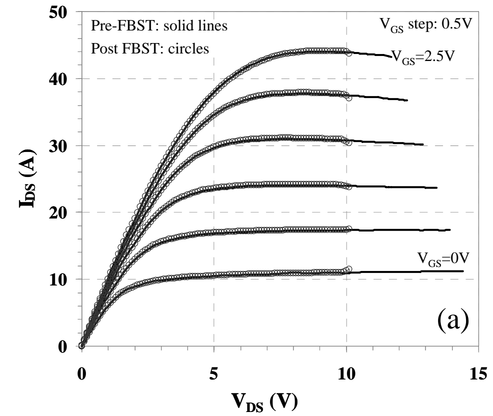

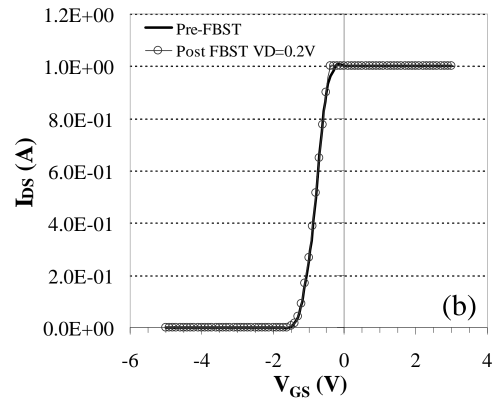

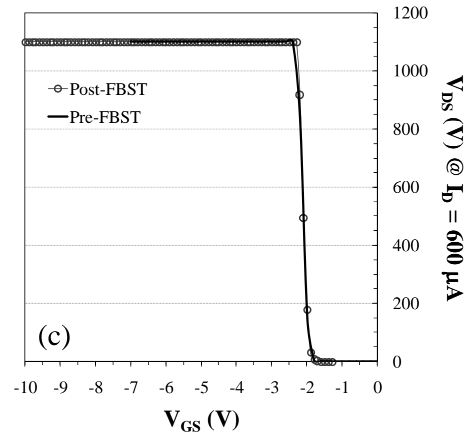

Fig. 4 (a) Forward, (b) transient, and (c) reverse characteristics of device W5-J1182 before and after the FBST at 200 °C for 112 hours.