

Inherently Safe Resonant Reset Forward Converter Using a Bias-Enhanced SiC JFET

R. Kelley^{1a}, T. Brignac^{2b}, M. Mazzola^{1c}, and J. B. Casady^{1d}

¹ SemiSouth Laboratories, Inc., 201 Research Blvd., Starkville, MS 39759 USA

² Mississippi State University Center for Advanced Vehicular Systems, 200 Research Blvd., Starkville, MS 39759 USA

^arobin.kelley@semisouth.com, ^btdb1@cavs.msstate.edu, ^cmike.mazzola@semisouth.com, ^djeffcasady@semisouth.com

Keywords: SiC, JFET, normally-off power switch.

Abstract. The power junction field effect transistor (JFET) is the second most mature SiC device, after the SiC Schottky diode, and is commonly associated with normally on functionality; but this feature is often viewed problematically for off-line dc-to-dc converter applications. Two inherently safe, single-switch dc-dc converter designs have been developed that put into practice pure SiC JFET devices (i.e., without cascoded devices) that possess enhancement-mode functionality and bias-enhanced blocking. These ‘Quasi-Off’ devices are designed to block half of the rated blocking voltage at zero gate bias and achieve full rated blocking voltage with a modest negative bias, typically between 0 and -5 V. Inherent safety is provided by utilizing the enhancement mode functionality of these devices as well as appropriate gate driver design. Bias enhanced blocking matches the dynamic stress encountered by modern high-frequency power supply topologies to the ratings of the device while recognizing that the larger dynamic stress is typically encountered only when the power supply (and especially the gate driver) is functioning properly.

Introduction

Many publications have previously reported the potential benefits of silicon carbide (SiC); i.e. higher blocking voltages, relaxed thermal requirements, and faster switching speeds. While the SiC JFET is the second most mature SiC device, it is perceived as a normally on device which has discouraged applications development. To overcome the normally on functionality, a cascoded device that uses a silicon MOSFET as the controlling switch in order to convert the normally on device to a normally off device has been reported [1]. While this configuration achieves that objective, the resulting device is still limited by the silicon technology and high packaging costs. The Si-SiC cascode does not allow designers to create new technology that fully benefits from the advancements that SiC technology can offer. The cascoded device can not be used for high temperature applications, or benefit from the scalability of SiC JFETs in parallel to form IGBT replacements with MOSFET switching properties.

To investigate an alternative solution, we have demonstrated a so-called quasi-off device whose characteristics are ideal for applications where the voltage stress on the switch has both a DC component and an added AC transient, which forms a large class of commercially important power electronics applications. This type of device is ideal for topologies such as the power factor correcting (PFC) boost converter, the classic hard-switched buck converter [3-4], and the resonant-reset forward converter that is the subject of this paper.

Device Functionality

A cross-sectional view of the VJFET device structure is shown in Fig. 1. The VJFET is device structure with a vertical channel and trench gates. The drain-to-source on-resistance threshold voltage, and channel punch-through voltage (which determines the blocking voltage at a given gate-source bias) is adjusted by adjusting the channel width and channel doping, among other variables. This ability to adjust the threshold voltage allows it to be shifted from negative to

positive values. Since the cut-on voltage for a SiC gate-source pn-junction is about 3 V, it is practicable to make the JFET either a normally on device, or a normally off device, or intriguingly, something in between [2]. Figures 2a and 2b compare the blocking voltage characteristics of a normally on and a quasi-off VJFET. The figures plot the maximum drain-source voltage (up to 600 V) that causes a drain leakage current of 100 μ A at the given gate-source voltage. As the gate-source voltage is swept from positive to negative, the result is a locus of blocking voltages (BV_{DS}) vs. V_{GS} . The blocking gain, which represents the differential improvement in blocking performance with added channel depletion arising from negative gate bias, is extracted from the linear portion of the curve and ranges from 50 with the normally on device to 300 for the quasi-off device. It is obvious from the plots that the threshold voltage for the normally on device is distinctly negative while for the quasi-off part it is slightly positive. This shift in threshold voltage allows the quasi-off device to block half the full rated blocking voltage (300 V) at $V_{GS} = 0$ V while achieving full rated blocking potential (600 V) at just a few volts negative on the gate. The quasi-off device is an optimal choice for applications where a normally off device is needed and a factor of two voltage derating is required, as well as applications where the switch must withstand a constant voltage stress applied by a DC source plus an AC transient experienced during normal operation. To address each of these rather general applications, a buck converter and a resonant-reset forward converter have been prototyped to demonstrate the practical benefit of the quasi-off device.

Applications

Previous work explains the design of an offline dc-dc buck converter (Fig 3) utilizing a quasi-off device [3-4]. For this design the quasi-off device provides the necessary isolation between the input and output by blocking the full-wave rectified 120-V AC line voltage ($V_{in} = 170$ V) at $V_{GS} = 0$ V. As normal switching action is initiated a negative voltage is applied to the gate

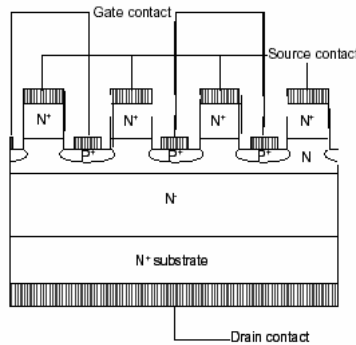


Figure 1. A schematic of a cross-Sectional view of a SiC JFET

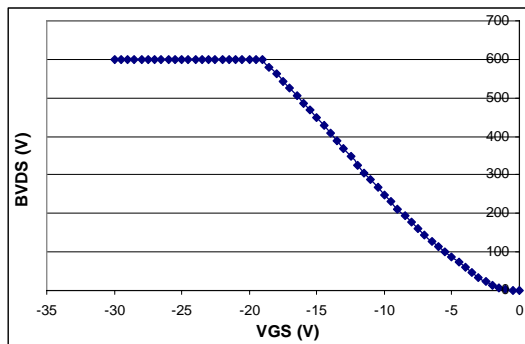


Figure 2a. BV_{DS} vs V_{GS} for Normally On VJFET

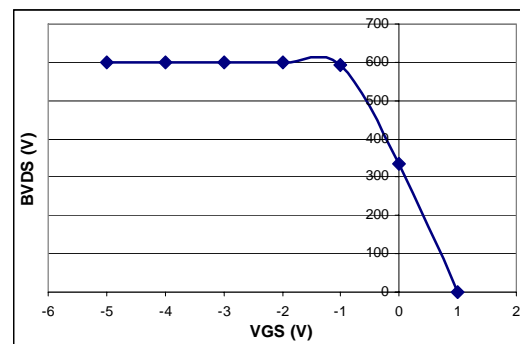


Figure 2b. BV_{DS} vs V_{GS} for Quasi-Off VJFET

during t_{off} that produces twice the blocking voltage, which is a more efficient solution than derating for providing the margin required by some standards. The VJFET acts as a normally off device blocking the full input voltage without a cascoded MOSFET.

Recent efforts have extended the buck converter to its transformer-isolated derivative in the form of a resonant-reset forward converter using a quasi-off pure SiC VJFET in contrast to previous work that used a Si-SiC cascoded device [1]. Figure 5a shows the inherently safe resonant reset forward converter design that provides a more efficient solution than a buck converter when large transformation ratios between input and output are required (typical of off-line power supplies) and/or transformer isolation is required.

This design has several features. First, by resonantly resetting the transformer, there is no need for a reset winding. Second, by using a transformer to provide the majority of the step down ratio, a more efficient voltage conversion is achieved because the duty factor can be optimally set by slightly adjusting the turns ratio. Lastly, and uniquely, the gate is magnetically driven allowing for the application specific integrated controller (ASIC) chip to be powered by the output. By including the ASIC on the secondary side, the use of an optocoupler for feedback is eliminated resulting in extremely reliable and convenient closed loop control. Directly powering the ASIC with the output ensures that the controller turns off in the case of a short circuit at the output. By design, the switch is rated to block the full DC input at zero gate bias, while gaining the ability to block the dynamic voltage stress experienced during normal resonant reset operation once the gate driver is started and a negative bias is derived on the bias capacitor. In the case of a gate driver failure, all dynamic stress ceases and the switch then blocks the dc input voltage indefinitely. A simple and low cost bypass resistor with capacitive isolation between the primary and the secondary will initiate start-up.

An offline to 24-V resonant reset forward converter was designed and prototyped using a 600-V, 3-A, quasi-off SiC VJFET exhibiting the blocking characteristics shown in Fig. 2b. Based on these characteristics, the switch can block the full rectified off-line input voltage at zero gate bias just as if it were a normally off switch. Once normal operation is initiated, a -5 V bias is generated by the gate driver that allows the device to block any resonant AC transients up to 600 V. Fig. 4b provides a PSPICE simulation of the prototyped design while Fig. 5b provides the measured results from the working prototype. The simulation and prototype results provide evidence of proof of principle and can easily be scaled to provide a high frequency, high power density solution in the kilowatt range.

Summary

A SiC VJFET that provides enhancement-mode functionality and bias-enhanced blocking gain without the use of a Si MOSFET cascode configuration is presented. This device is an ideal solution for applications that could benefit from SiC but require inherent safety. Two general

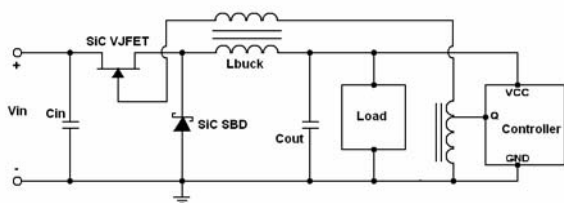


Figure 3a. An inherently safe buck converter design using a quasi-off SiC VJFET [3].

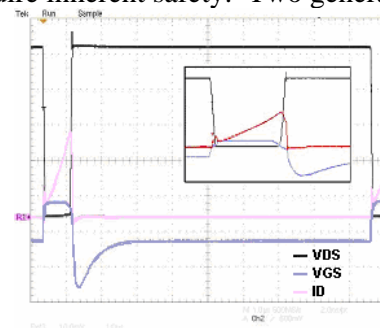


Figure 3b. V_{DS} , V_{GS} , I_D , and V_{out} for buck converter design.

$V_{in} = 170 \text{ V}$, $V_{out} = 12 \text{ V}$, $f_s = 100 \text{ kHz}$.

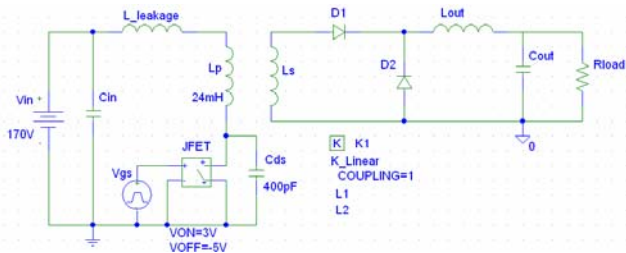


Figure 4a. PSPICE schematic of the resonant reset forward converter. $L_{\text{leakage}} = 10 \mu\text{H}$.



Figure 4b. Simulation results. $V_{\text{in}} = 170 \text{ V}$, $V_{\text{out}} = 24 \text{ V}$, $f_s = 50 \text{ kHz}$.

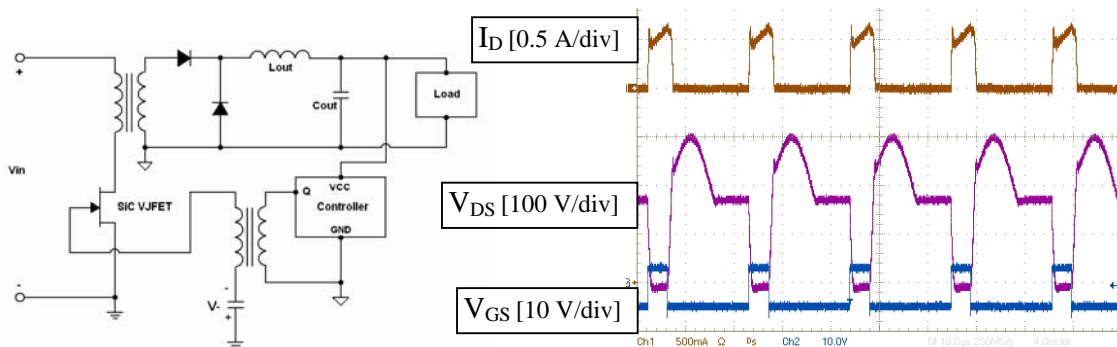


Figure 5a. An inherently safe resonant reset forward converter design using a SiC VJFET.

Figure 5b. V_{DS} , V_{GS} , and I_{D} for resonant reset forward converter design. $V_{\text{in}} = 170 \text{ V}$, $V_{\text{out}} = 24 \text{ V}$, $f_s = 50 \text{ kHz}$.

applications for the quasi-off device were presented. The general nature of similar application circuitry indicates that there are many other application opportunities. The quasi-off SiC VJFET provides a superior alternative to the MOSFET by providing normally off functionality with gate driver requirements consistent with the low digital control voltages currently used. The MOSFET typically requires a large gate voltage (15 V and greater) and high peak gate charging currents. In contrast, the quasi-off SiC VJFET can be controlled over a range from -3 V to +3 V. Finally, the SiC JFET with vertical channel inherently offers lower specific on-resistance than a MOSFET.

Acknowledgement

This work was supported by contract F33615-01-D-2103 and managed by Dr. James Scofield, in the Propulsion Directorate of the Air Force Research Laboratory.

References

- [1] J. M. Hancock, "Meeting Future Application Challenges in HV Semiconductors," Infineon Technologies, Invited Presentation at IEEE APEC 2004.
- [2] M. Mazzola, J. B. Casady, N. Merrett, I. Sankin, W. Draper, D. Seale, V. Bondarenko, Y. Koshka, J. Gafford, and R. Kelley, "Assessment of 'Normally On' and 'Quasi On' SiC VJFET's in Half-Bridge Circuits," *Mater. Sci. Forum*, Vols. 457-460, pp. 1153-1156, 2004.
- [3] R. Kelley, M. Mazzola, W. Draper and J. Casady, "Inherently Safe DC-DC Converter Using a Normally-On SiC JFET," IEEE APEC 2005. Volume 3, 6-10 March 2005, Page(s):1561 - 1565.
- [4] M. Mazzola and R. Kelley, "Inherently Safe Buck Converter Design for the SemiSouth Silicon Carbide HEL²FETTM," Applications Note, March 2005.