

Inherently Safe Buck Converter Design for the SemiSouth Silicon Carbide HEL²FET™

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I. Introduction

The power junction field effect transistor (JFET) is commonly associated with normally on functionality, which is often viewed as being problematic for off-line dc-to-dc converter applications. In this applications note, we illustrate an inherently safe off-line buck converter that has the following features:

- Fully self-starting without electronic or mechanical relay disconnect.
- Indefinite short circuit protection.
- Inherently safe in case of gate drive failure.
- MHz switching performance.

The example design captures the benefits of SemiSouth's HEL²FET™, a SiC power JFET. The circuit is inherently safe in part because of the Enhancement-mode functionality and bias-enhanced blocking voltage of the HEL²FET™. In addition, the circuit has:

- Low part count.
- Galvanic separation of the input and the output when off.

A single-switch 500 to 1000 W off-line dc-dc converter is a cost effective option for generating quasi-regulated dc bus voltages for use in distributed power architectures (DPA), such as in a concentrated server or telecom switch installation. For example, consider Fig. 1, which illustrates a two-converter combination involving a boost converter for power factor correction (PFC) and a buck converter for stepping down the 300-V dc voltage resulting from boosting full-wave rectified, neutral-referenced, line-to-

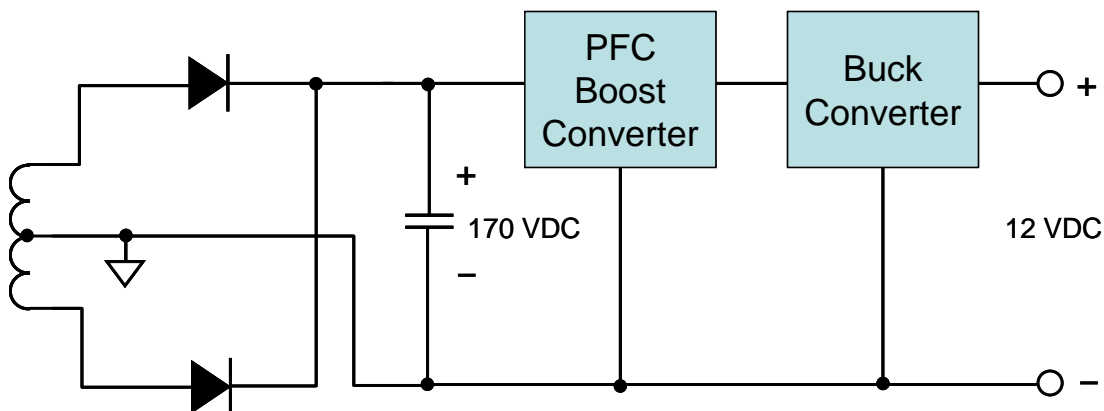


Figure 1. Example off-line power supply for a 12-V dc distribution bus. A standard neutral-referenced 240-VAC utility supply provides a grounded, touch-safe common rail.

line 240-VAC (120 VAC-neutral-120 VAC) utility power. Thus, the common rail of both the PFC front end and the step-down buck converter are bonded to the building neutral, which ensures that the common is referenced to a safe ground potential at all times. Alternatively, the step down stage can be a classic transformer-isolated dc-dc converter (e.g., either conventional forward or resonant reset). The latter case will be addressed in a separate applications note. The design example given here will focus on the buck converter operating stand-alone without a PFC front end. The methods described apply equally well to the boost converter stage used for power-factor correction.

II. Enhancement-Mode HEL²FET™

The HEL²FET™ is available with Enhancement-mode functionality and bias-enhanced voltage blocking. This means that the device will block 50% of its voltage rating at $V_{GS} = 0$ V, and 100% of its voltage rating at a modest negative gate-source bias of -5 V. This unique design eliminates the possibility of shorting the dc input rail during start-up, gate driver failure, or output short circuit conditions.

A. Buck Converter Design

Figure 2 illustrates a 170-V to 12-V buck converter utilizing the Enhancement-mode HEL²FET™ in the high-side position. Thus, the bonding of the common rail to the building neutral (and thus the building safety ground) is guaranteed at all times. A secondary winding is added to the buck converter inductor to dynamically float the gate potential to the reference source potential [1]. A typical buck converter controller chip,

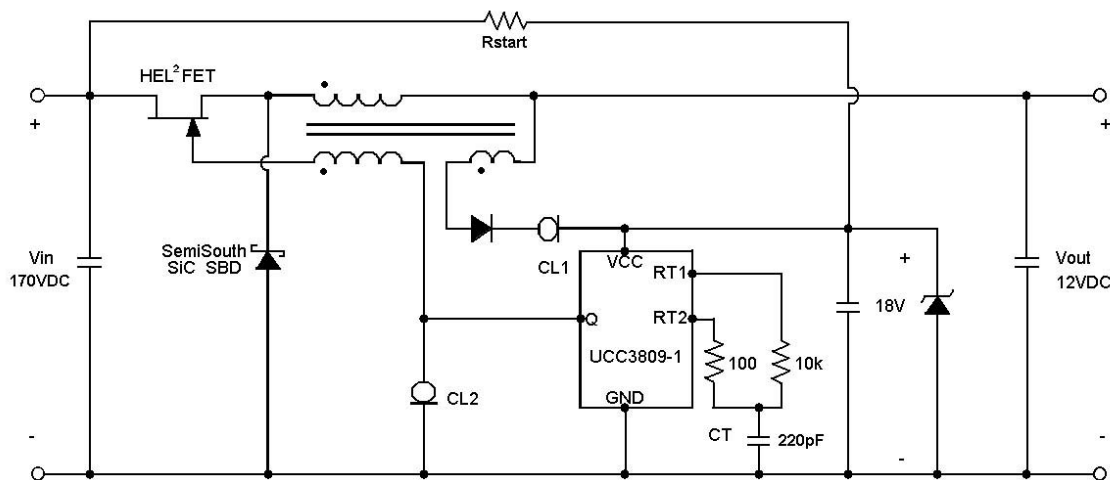


Figure 2. Inherently safe dc-dc buck converter with Enhancement-mode HEL²FET in high-side switching position. Feedback network for closed-loop voltage regulation not shown.

referenced to the supply common, is assumed to have the typical silicon MOSFET gate drive capability, which is more than sufficient to drive the HEL²FET's™ low gate charge. The controller chip is powered by a series combination of the 12-V output and an additional 5 V derived from a single-turn auxiliary winding added to the buck inductor ($V_{CC} = 17$ V). The output of the chip, then, will always produce a +3 V margin over the



output voltage, which ensures that the transistor receives the positive gate-source bias required to drive the HEL²FET™ to minimum on-resistance. During the off period, the controller chip output returns to zero, which simultaneously biases the transistor to $V_{GS} = -V_{out} = -12$ V because the source terminal floats with the output voltage. Since the Enhancement-mode HEL²FET™ can block the full dc input voltage at $V_{GS} = 0$ V, start-up is inherently safe. However start-up is not automatic unless a bypass resistor is included which charges the controller-chip's V_{CC} filter capacitor from the input filter capacitor until the chip begins to oscillate; at which time the transistor will charge the output filter capacitor and sustain the controller chip continuously.

A 500-W circuit design, based on the methodology documented in [1], has the following features:

- $V_{in} = 170$ VDC (full-wave rectified 120 VAC)
- $I_{in} = 4.6$ A @ 90% efficiency
- $V_{out} = 12$ VDC
- $I_{out} = 41.7$ A
- $f_s = 1$ MHz
- Duty Factor ~ 10%
- Buck Inductor = 1.3 μ H
- Inductor current ripple = 8.3 A (20%)
- Peak inductor current = 50 A
- Output filter capacitance ≥ 2.2 nF

Figure 3 illustrates the operation of a representative converter built with an Enhancement-mode HEL²FET™. Due to limitations on the minimum pulse-width available from the UCC3809-1 ASIC, operation was limited to $f_s = 512$ kHz. The switching speed of the HEL²FET™ is less than 50 ns, and the resulting converter waveforms illustrate that the HEL²FET™ could easily support a 1-MHz switching frequency at the very low duty factor required for the 10:1 step-down ratio. A SemiSouth SiC Schottky barrier rectifier provides the free wheeling rectifier function, which further enables efficient high-frequency operation of the converter. Note that in Figure 3, as the continuous inductor current is commutated to the switch, a displacement current pulse is observed at turn-on that charges the normal Schottky depletion capacitance; which amounts to a total charge of 10-20nC for the SemiSouth SiC Schottky rectifier. Since the free wheeling diode is a Schottky rectifier, not a p-n diode, there is no other reverse recovery transient.

B. Short-Circuit Operation

A hard short circuit of the output will rapidly cause the chip to stop oscillating as V_{CC} declines without replenishment from the output. When the chip stops oscillating, the HEL²FET™ resumes blocking as though start-up conditions have been re-established, and the short-circuit is automatically and safely disconnected from the input voltage supply. From time-to-time, the start-up bypass resistor will create a burst of pulses that the transistor will respond to by switching a few pulses into the inductively limited short circuit. The bypass resistor should be set large enough to generate such pulses at a low repetition frequency (a few Hertz). When the short circuit is cleared, the power supply will restart normally.

$$T_{case} = 225^{\circ}\text{C}$$

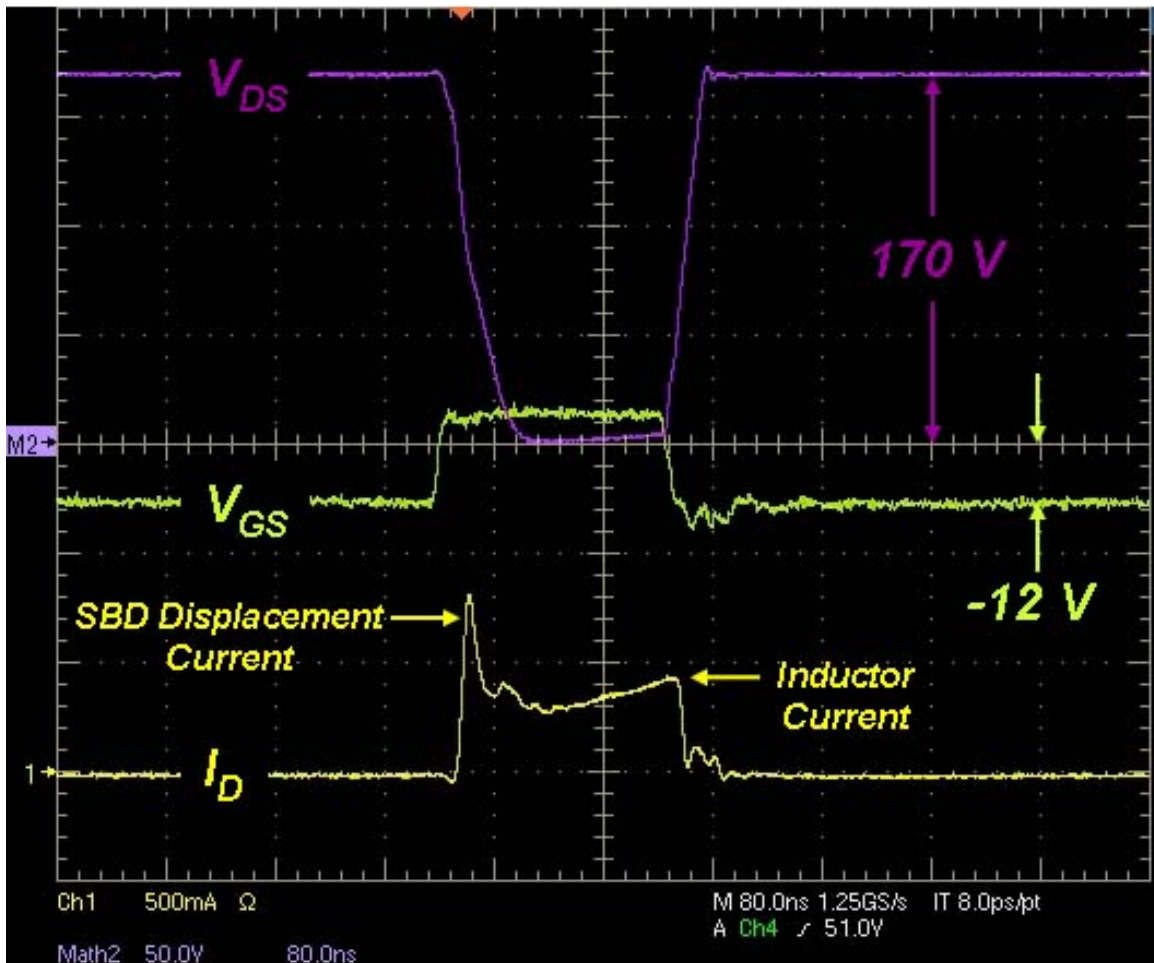


Figure 3. Representative waveforms for the HEL²FET™ transistor switching at a 50% duty-factor equivalent switching frequency of 2.5 MHz. The buck converter is running at 512 kHz. The transistor case temperature $T_{case} = 225^{\circ}\text{C}$.

C. Gate Driver Failure

There are two forms of gate driver failure considered here: “Stuck Low” and “Stuck High.” Since the controller chip is the only active device connected to the gate of the transistor, Stuck Low means a constant zero output voltage from the chip. Stuck High means a constant output voltage from the chip equal to V_{CC} . Since, as will be shown, Stuck High is a special case of Stuck Low, Stuck Low is treated first.

When the chip output is stuck low, $V_{GS} = -V_{out}$ which forces the transistor to turn off and block the input voltage until the gate driver begins oscillating again. If the failure is permanent, then the Enhancement-mode HEL²FET™ will safely maintain the quiescent condition indefinitely even if the output voltage decays to zero.

When the chip output is stuck high, initially $V_{GS} = -V_{out} + V_{CC} \approx +3 \text{ V}$. Thus the transistor will conduct more current to the output filter capacitor than required by the load



and the output voltage will begin to rise. But since V_{CC} is clamped by a zener diode, the additional voltage is dropped across the current limiting diode CL1. Thus the output voltage increases only 3 V before the transistor returns to cutoff conditions ($V_{GS} = 0$) and the output voltage stops rising. The second current limiting diode, CL2, guarantees that the gate voltage will be clamped to ground in case of an open-circuit failure in the output of the controller chip. The current limit for CL2 is selected to be greater than CL1. This ensures that under Stuck High conditions the V_{CC} filter capacitor must discharge when the transistor is pushed into cutoff by the rise in the output voltage. Under normal operating conditions the average current shunted to ground by CL2 is reduced by the duty factor (10% or less), while CL1 continuously replenishes the V_{CC} filter capacitor. Excess current from CL1 is shunted by the zener diode clamping V_{CC} . A design equation that ensures more than adequate replenishment of charge to the V_{CC} filter capacitor during normal operation, but a definite transition from Stuck High to Stuck Low conditions under abnormal operation is $I_{CL2} \approx 3I_{CL1}$. As has already been discussed, the Enhancement-mode HEL²FET™ will safely block the input voltage under the Stuck Low condition indefinitely.

III. Scaling

The SemiSouth HEL²FET™ featured in the experimental results of this applications note conforms to the current version of the HEL²FET™ data sheet [2]. This part is available by custom order in current ratings up to an $I_{DSS} = 40$ A, which will satisfy

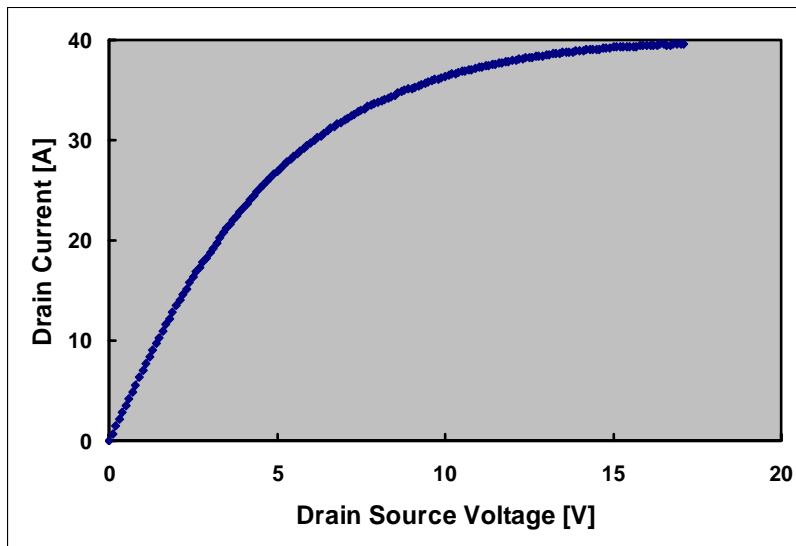


Figure 4. SemiSouth HEL²FET™ with $I_{DSS} = 40$ A at $V_{GS} = +2$ V.

scaled versions of this application up to the design featured in section II A. A typical drain characteristic for the high-current version of the HEL²FET™ is shown in Figure 4. Contact SemiSouth sales engineering at will.draper@semisouth.com for ordering information.

IV. References

[1] R. Kelley, M. Mazzola, W. Draper and J. Casady, "Inherently Safe DC-DC Converter Using a Normally-On SiC JFET," in *Proc. of IEEE APEC*, paper D4.4, 2005.

[2] HEL²FET Preliminary Data Sheet #HLF0602T1 Rev. B, SemiSouth Laboratories, Inc.